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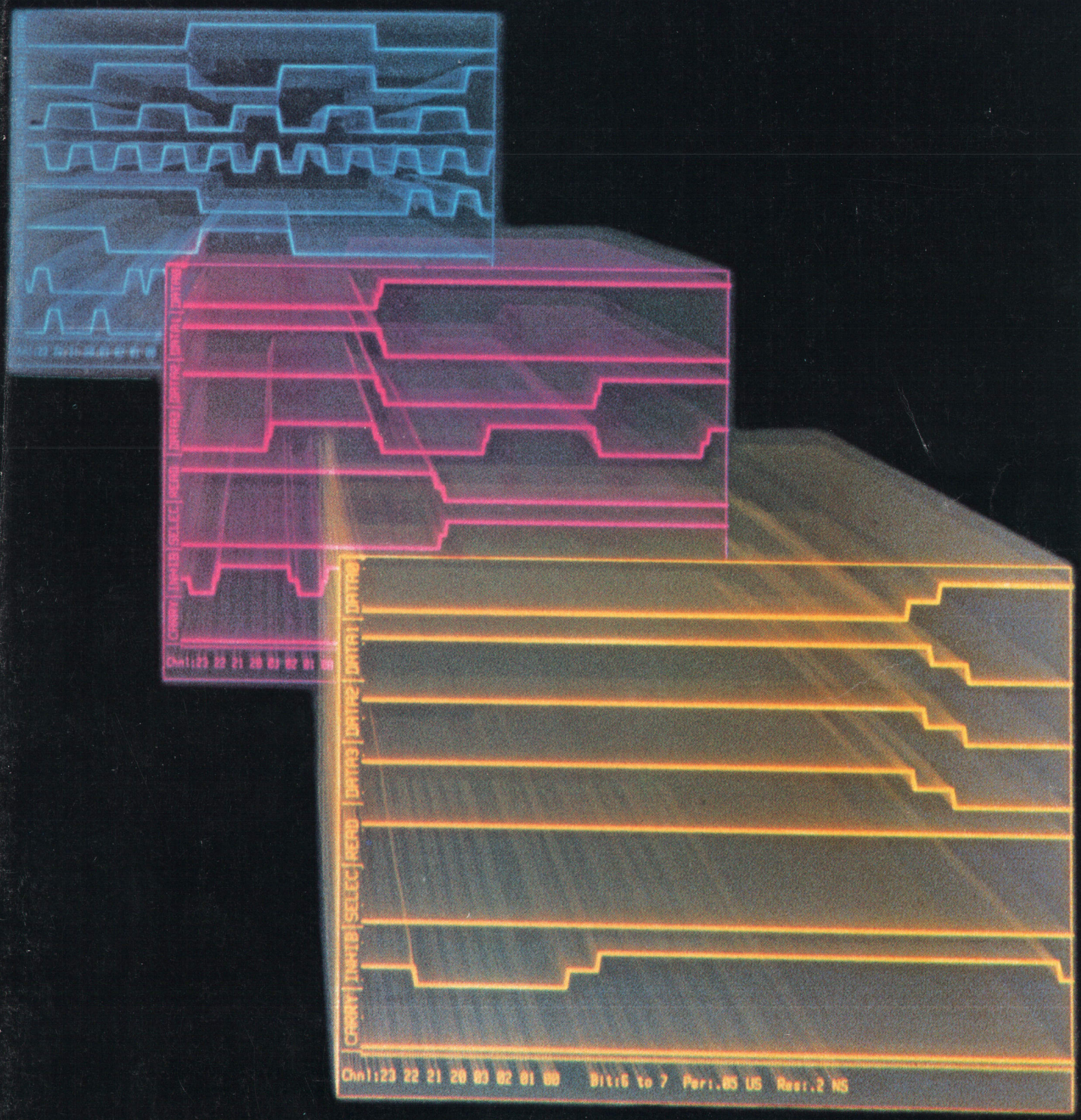
HEWLETT-PACKARD JOURNAL



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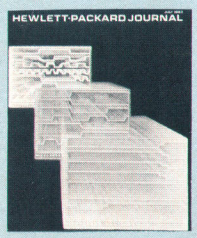

Quality is high on everyone's priority list these days, and one of the principal paths to quality is testing, thorough and realistic, at all phases of the process of designing and producing a product. This month's issue deals with two families of test instruments that are aimed at assuring the quality of the myriad diodes, transistors, resistors, capacitors, inductors, integrated circuits, circuit boards, and modules that go into electronic equipment. Each family has a target range of testing applications and a repertoire of special capabilities needed in those applications.

On this month's cover are three views, at progressively finer resolution, of the timing diagram of a RAM (an integrated circuit random-access memory chip). Memory circuits like this one, along with microprocessors, gate arrays, and other digital integrated circuits (ICs) are becoming faster and more complex at a startling rate—sometimes the next generation is announced before its predecessor is in production. The system that produced this timing diagram is designed to keep up with the rapidly changing state of the art and to test fast, complex digital ICs at realistic speeds and in minute detail. This family of instruments, consisting of the 8180A Data Generator, the 8181A Extender, and the 8182A Data Analyzer, is distinguished by a time resolution of 100 picoseconds (there are a million picoseconds in a millionth of a second) and the analyzer's programmable sampling point delay. These features make it possible to zero in on the briefest of IC events. You can read all about the design of this system on pages 3 to 31.

While the 8180A/81A/82A System is designed for relatively low-volume testing of complex, high-performance digital ICs in engineering, quality assurance, depot maintenance, and certain kinds of incoming inspection and production testing, the 4276A and 4277A LCZ Meters are aimed mainly at high-volume incoming inspection and production testing of discrete components (LCZ stands for inductance-capacitance-impedance). They also have their uses in the engineering laboratory and in semiconductor evaluation. By testing components faster and more realistically than previously available equipment, these instruments improve the quality and lower the cost of the products we purchase. Fed by an automatic component handler (available from several manufacturers), they'll check up to ten components per second and sort them into as many as ten classes, and keep it up hour after hour without attention. For reporting test data, they're compatible with computers and plotters, and for realistic testing, they offer a variety of test frequencies and voltages. The designers tell their story on pages 32 to 38.

-R.P. Dolan

A High-Speed System for AC Parametric Digital Hardware Analysis

This new 50-MHz stimulus-response system is a state-of-the-art tool for comprehensive and rapid characterization of all types of digital circuits.

by Andreas Wilbs and Klaus-Peter Behrens

RAPIDLY ADVANCING SEMICONDUCTOR technology now makes it possible to integrate thousands of functions on a single chip, making digital circuits increasingly more complex. They are also getting faster. Subnanosecond propagation delays per gate are already feasible, allowing clock rates of 50 MHz and higher even for complex devices. Furthermore, new circuit designs, both custom and semicustom (gate arrays), are receiving broad acceptance in the marketplace.

This evolution has changed the requirements for digital test equipment. The most significant new requirements are:

- Higher data rates and more channels
- More accurate timing and stimulus/comparator levels
- A capability for longer test patterns.

It is also important for instrumentation to be compact, quick to set up, and adaptable to different devices and measurement problems.

Traditional measurement solutions do not fulfill these new requirements. Big expensive test systems, for example, are well suited to dc parametric tests and provide high production throughput, but for low-volume engineering applications, they are seldom readily available, and most are too slow for testing fast devices at speed. The lack of a live keyboard and difficult operating and programming procedures make such systems inflexible and prevent the quick access necessary in a laboratory environment. Another traditional solution is the self-configured, dedicated setup containing several word/pulse generators for stimulus, and logic analyzers, counters, and oscilloscopes for analysis. Programming these different instruments requires long familiarization, and synchronizing the setup is difficult and time-consuming.

The New Solution

The new HP 8180A/81A/82A Stimulus/Response System (Fig. 1) provides an answer to the new requirements. It offers both device stimulation and response analysis, and consists of the 8180A Data Generator, the 8181A Extender,

Fig. 1. *The 8180A Data Generator (top left), the 8181A Extender (not shown), and the 8182A Data Analyzer (bottom left) provide high-performance, easy-to-use, economical at-speed testing for digital integrated circuits, boards, and modules. The system can be controlled by a desktop computer (right) via the HP-IB (IEEE 488).*

Parametric Characterization of Digital Circuits

The representative timing parameters of synchronous ICs are setup time, hold time, and propagation delays. During the setup and hold times, data has to be stable before or after an active clock transition occurs. The propagation delay is the time between stimulation and the output reaction of a device. This value depends upon the complexity of the circuit and its technology, and varies from less than 1 ns for an ECL gate to over 100 ns for an MOS gate. Hence, the measuring instrument must have high timing resolution. In addition, these timing parameters depend on the dynamic input characteristic of a device. For example, the reaction time of a comparator depends on the input overdrive.

At the output of the device under test, the variation of amplitude with frequency is of interest. A driver may have the ability to deliver adequate dc current under the specified fanout conditions, but be unable to deliver adequate peak current to drive the parasitic capacitance at high clock rates.

Applications of the New System

The 8180A/81A/82A System is oriented predominantly towards the solving of engineering measurement problems. IC and board designers need to measure parameters to specify the performance and optimize the yield of ICs, or achieve a high turn-on rate of boards. Digital IC manufacturers do parametric characterization of ICs in the prototype phase, allowing the process to be optimized. They also use parametric analysis to establish sales specifications and for in-depth evaluation in the quality assurance department.

The 8180A/81A/82A System's main applications for digital circuit, module, and system manufacturers are found in R&D, production engineering, quality assurance, incoming inspection, and materials engineering. For example, various propagation delays must be matched for minimum skew. Logic functions must be verified. A stimulus is required to simulate the interface pattern of a board that is not yet built. Parametric circuit test at the board level has the same requirements and objectives as at the IC level, differing in complexity and error sources. The cross talk on a bus with parallel lines or data stability during the time window around the system's synchronous clock are of interest. Other applications include low-volume and at-speed testing in production, incoming inspection, and depot maintenance, where traditional equipment such as board testers offers insufficient speed and timing performance. High-reliability applications, such as aerospace equipment, also demand a 100% parametric test in addition to detection of soldering and component loading errors. Component approval and production engineering departments are also application areas for the new system.

which expands the number of stimulus channels, and the 8182A Data Analyzer. Each of the units can be configured for different numbers of channels. In addition, provision has been made for the synchronous operation of two systems in parallel. This expands the channel count with a minimum of skew. Generator/analyzer synchronization and interaction with the device under test are assured by various control inputs and outputs. Adaptability and clean signals are provided by a range of useful accessories.

Although the instruments are designed as a system and offer the same key specifications, the 8180A (with or without the 8181A) and the 8182A can also be operated individually. Each unit has its own control processor, display, keyboard, and HP-IB (IEEE 488) interface. This modular concept makes the instruments very adaptable to different devices and measurement problems.

This compact system brings the performance of a big tester to the bench. Its user-oriented softkey operating concept speeds the setup of timing and level parameters, either manually or under HP-IB control. The same is true for test pattern creation, which is further simplified by standard data patterns and pattern editing features.

Modularity gives the user the means to adapt a system exactly to requirements, thus keeping the cost low enough to justify the expense. This is important in low-volume testing, where the return from high throughput found in production areas is not achieved.

The need for high speed is satisfied by the system's 50-MHz data rate. This is faster than most of the big IC testers and covers most applications, bearing in mind that the overall speed of a device is much slower than a single gate delay. The rate slows with increasing complexity, so that even fast ECL devices can be tested by the system. In addition to a fast rate, sophisticated timing capabilities are provided for setting up various test patterns for an IC. The stimulus channels provide independent delay and data width programming, with excellent resolution of 100 ps for very tight adjustments. Operation of the 8182A Data Analyzer is mostly synchronous, a technique similar to that employed by more expensive IC test systems. It is capable of both synchronous (external clock) and asynchronous (internal clock) operation, and it also offers 100-ps resolution, never previously achieved in an asynchronous analyzer. When the device under test and the analyzer are synchronized, automatic comparison of sampled data with expected data is possible. The 8182A's threshold level range is sufficiently wide to test all common logic families, and logic levels are independently adjustable for mixed logic circuits. The level resolution is 10 mV.

Data Generator Provides Stimulus

The 8180A Data Generator outputs a digital data pattern according to the user's specifications, which may include data rate, bits per word, number of data words, levels, timing relationships between channels, and other parameters. The data generator contains the following basic blocks:

- Timing circuits to achieve specific timing relationships between channels
- Memory to hold the data pattern that is to be output in parallel
- Output amplifiers that determine the output voltage swings
- Control inputs and outputs
- Central processor unit
- HP-IB interface
- Keyboard and display.

An add-on unit and pods provide for three-state operation with programmable levels for testing bidirectional buses.

The 8180A is designed to be the stimulus for parametric

hardware analysis. Therefore, it provides precise level and timing capabilities at high speed. This is in contrast to other types of word generators, which often provide data patterns only at low speed, with moderate or no level definition and poor timing capabilities.

The 8180A can be configured as an 8-to-16-channel generator in 4-channel increments. A maximum of eight channels can be RZ (return to zero), that is, having independently programmable delay and width. All other channels are NRZ (non return to zero) channels. The channel count can be expanded by using up to two 8181A Extenders, each with a maximum of 24 NRZ channels with programmable common delay. This configuration provides 64 channels. Synchronous parallel operation doubles this number to 128.

Data Analyzer Measures Response

The 8182A Data Analyzer collects, analyzes, and displays digital bit patterns. These tasks are performed according to the user's specifications, which may include input thresholds, data qualification, sampling point (the point in time at which data is sampled, referenced to the external clock), compare time window, and other parameters. The 8182A contains the following basic blocks:

- Input comparators to determine the states of logic signals (1, 0, or between high and low thresholds)
- Trigger circuits to indicate the beginning or end of data capture
- High-speed memory to store sampled data
- Low-speed memory to hold reference data
- Timing circuits to determine precisely when data is to be captured or compared
- Control inputs and outputs
- Central processor unit
- HP-IB interface
- Keyboard and display.

The 8182A Data Analyzer is designed for high-speed functional and parametric hardware analysis of digital circuits. The data analyzer can be configured from 8 to 32 channels in 8-channel increments, each channel having identical analyzing capabilities. Synchronous parallel operation doubles the number of channels to a maximum of 64.

User-Friendly Operation

The 8180A Data Generator and 8182A Data Analyzer are designed to fulfill the requirements of digital circuit hardware analysis. For this reason the usual data generator and logic analyzer concepts have been replaced by a new operating concept tailored to this application. The design goals for this new concept were:

- Fast, guided setup of the instrument, thereby dispensing with the operating manual in a relatively short time
- Parameter changing during the instrument's active state (live keyboard)
- Comfortable data loading, edit, and display features
- Simple HP-IB programmability for fast program generation
- Similar operation of both instruments.

To reduce the number of keys and the confusing use of shift keys, a layered menu softkey concept was chosen. The display is divided into three areas (see Fig. 2). The top of the screen next to the **OPERATION** keys gives status information. (These keys operate independently of all other keys on the front panel). The remainder of the display is split into a report area, showing one of seven selectable reports

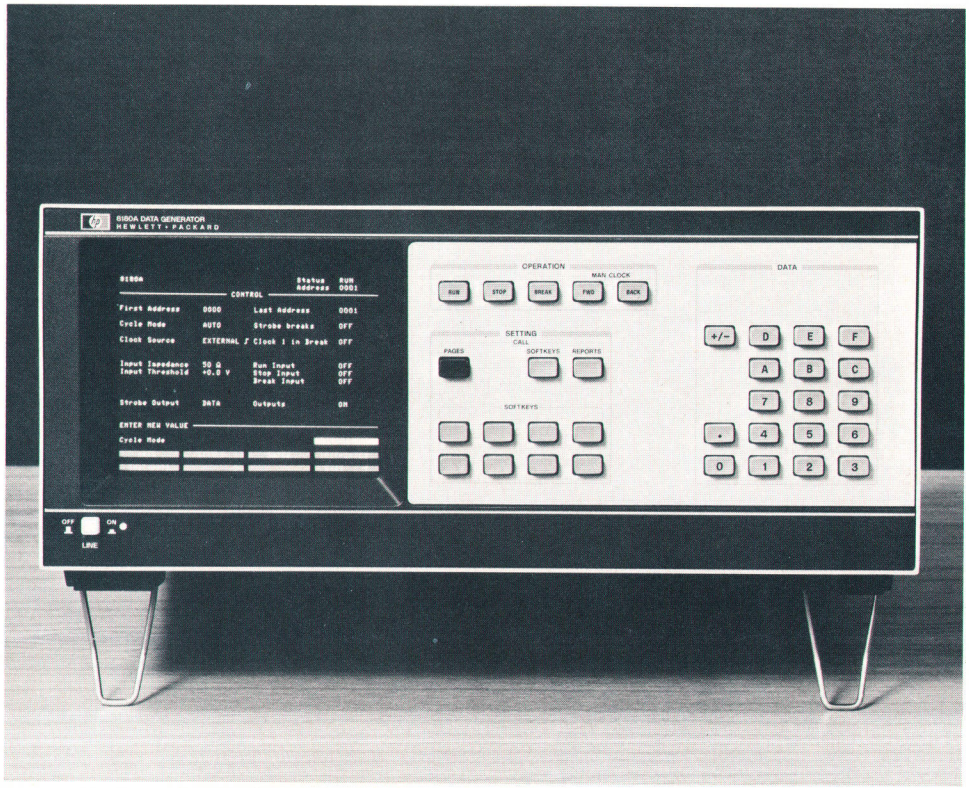

Fig. 2. *The 8180A Data Generator and the 8182A Data Analyzer have similar operating concepts, displays, and front panels. The display is divided into status, report, and softkey areas.*

(parameter settings or data display), and the softkey area containing the entry field, which shows the selected parameter and the labels for the eight softkeys beside the screen. Softkey and report areas can be selected independently or in common by the **CALL** keys. If the entry field is not activated, the area can be used to extend the data display in the report area. The parameters are selected by the softkeys either directly (e.g., softkey label Cycle Mode to access the cycle mode), or through a softkey tree (e.g., softkeys Trigger and Delay lead to trigger delay). After selection, the parameters can be changed either by softkeys or by data keys. Any softkeys that contribute nothing to the current operational status of the instrument are blanked to avoid confusing the user.

This operating concept offers quick access to every parameter, regardless of the contents of the report area.

Similar Operation

The 8180A Data Generator and 8182A Data Analyzer are designed to operate similarly, so that a user who is familiar with one instrument can use the other without a long familiarization time. The keyboards differ in only three keys. Softkeys with the same function for each instrument are labeled identically and occupy the same position on both keyboards (many softkey label sets on both instruments are identical). The pages displayed are very similar, too, with main settings shown on the control page. The timing parameters, which appear on the analyzer's control page, require a page of their own in the generator. The generator's output page corresponds to the analyzer's input page in the same way the 8180A output data page corresponds to the 8182A expected data page.

Both instruments have a miscellaneous page, which in the 8182A also contains store and recall functions. A special feature of the generator is the macro data page, which extends considerably the editing capabilities of the instrument. The data analyzer has three pages on which to display received data in the form of the state list, the timing diagram, and an entirely new feature called the error map. The error map gives a concise overview of the Compare Data result. It displays one dot for each memory location. This dot is replaced by a square if data received differs from expected data. Furthermore, there are special features for the individual masking of any bit or word (see article, page 14).

The expected data page, the state list, and the data page in the 8182A are user-defined. Channels can be deleted from the display or grouped together in segments of up to 16. The channels in each segment can be configured in a manner that is totally independent of their hardware order, enabling the user to assign a code to every segment. It is also possible to display a channel in more than one segment concurrently. The timing diagram offers a full set of features, such as zooming in both horizontal and vertical axes, glitch display, delta measurement, and individual channel arranging.

Special attention was paid to the editing features. The 8180A has memory, line, and channel editing features. Memory editing consists of set and clear functions. Channel editing provides clear, set, counter, PRBS (pseudorandom binary sequence), and copy. Line editing functions include insert, delete, copy, and move. It is also possible to define a set of 16 words (macros) on a special page, and then copy one or more of them to the data memory.

In addition to many of the above features, the 8182A has other analyzer-oriented editing features for expected data. These include the setting and clearing of masks, and the ability to copy received data to the expected data memory for future comparison.

Live Keyboard

For fast parametric measurement it is often necessary to change instrument parameters during the measurement phase. In the 8180A this is achieved by changing all analog parameters without disturbing the generator output in any way. If other changes (e.g., output data) are being made, the instrument interrupts the cycle to make the change, and then returns to the point at which the cycle was interrupted.

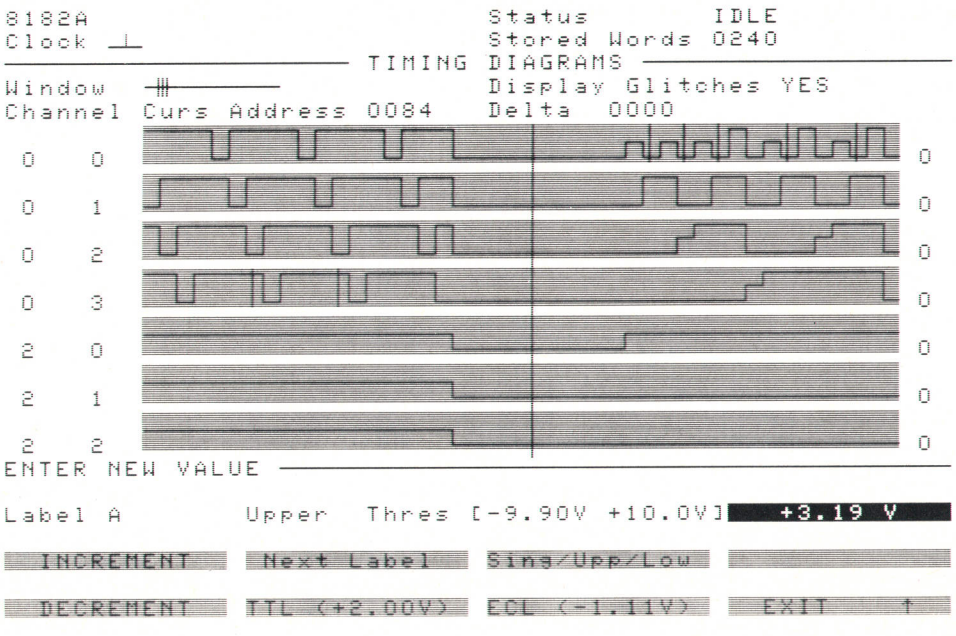

Fig. 3. *When changing measurement parameters during a measurement, the display can be split into two areas, one of which shows control page parameters in the softkey area. Here the timing page is displayed while the probe threshold is being changed.*

This operation is performed without disturbing clocks or data. Therefore, the device under test, which contains only combinational and sequential logic, does not recognize the interruption.

The 8182A Data Analyzer's input thresholds can also be changed during the active cycle (data capture). Other analyzer features facilitate fast measurements. The microprocessor displays the received data not only when the instrument stops, but also when the data rate falls below 10 MHz. This is a particularly useful attribute when dealing with slow clock rates or clock bursts. Other instruments usually have to abort a measurement to display the data received. Another useful feature is auto-arming. This allows the user to preselect the point in time at which the instrument will begin a new measurement, so that the result of any change in the operating condition of the device under test can be displayed immediately.

To ensure that the instrument is operable during a period of processor activity, the keyboard is interrupt-controlled, permitting the storage of up to eight keystrokes until the processor has time to respond to them. When changing measurement parameters during a measurement phase, it is possible to split the display screen into two areas, one showing the report area (perhaps the error map), and the other showing control page parameters in the softkey area. Fig. 3 shows an example; the timing page is displayed while the probe threshold is being changed.

The HP-IB system is designed to give direct access to parameters and a fast instrument response. The mnemonics are easy to remember, avoiding the need to refer to the manual continuously, making programming simple and reducing familiarization time. To program the 8180A to a frequency of 20 MHz, for example, the controller sends the message FRQ 20 MHZ. Where the parameters on each instrument are identical, so are the mnemonics.

For the transfer of high volumes of data from the controller to the instrument and vice-versa, a binary transfer mode has been implemented. In this mode, every byte on the bus is dedicated to eight bits of data. Data transfer rates of 12,000 bytes per second are achieved, giving a data reload time of less than two seconds for the whole system. This makes it possible to write fast-running programs.

Acknowledgments

We would like to thank Roberto Mottola for his outstanding contribution in defining the operating concept for both instruments, Horst Link, who was responsible for the mechanical design of all instruments and accessories, Eckhard Hettlage, who designed the displays, Peter Stollenmaier, who contributed to the 8182A power supply, Rainer Storn, who helped with the 8182A self-test software, and last but not least, our thanks go to Günter Riebesell and Reinhard Falke for their help and guidance along the way.

A High-Speed Data Generator for Digital Testing

by Ulrich Hübner, Werner Berkel, Heinz Nüssle, and Josef Becker

THE NEW HP 8180A DATA GENERATOR represents a significant step forward in the production of high-speed data generators. It offers high timing accuracy, precise pulse-level definition, ease of operation with either manual or remote control, and great flexibility on the bench and in the rack.

The 8180A consists of a power supply module, a display module, and eleven printed circuit boards, which plug into a motherboard. Fig. 1 illustrates the various functional blocks and main interconnections.

The 8181A Data Generator Extender is constructed along the same lines as the 8180A with the exception of the display and keyboard. All control functions are performed by the 8180A, the 8181A being merely a system slave. Fig. 2 is a block diagram of the 8181A.

Internal System Organization

All high-speed control signals in the 8180A Data Generator are generated on two boards, designated Address Control 1 and Address Control 2 (ADC1 and ADC2). The logic consists of 10k and 100k ECL devices and is controlled by the central processing unit by way of a high-speed bidirectional bus.

On ADC1, three signals that synchronize the address counters and signals for both clock channels are generated. The board responds to the commands RUN, GATED, STOP, and BREAK. There are three basic operating modes:

- Single cycle: a RUN signal starts a single cycle from the preset first address to the preset last address.
- Auto cycle: after a RUN signal, data is generated repetitively from the first to the last addresses.
- Initialization and auto cycle: a RUN signal starts data generation at address 0000. Data generation continues to the first address and then cycles between the first and last addresses repetitively.

In these three operating modes, cycling is halted on receipt of a BREAK or STOP signal.

Two further modes are controlled from this board:

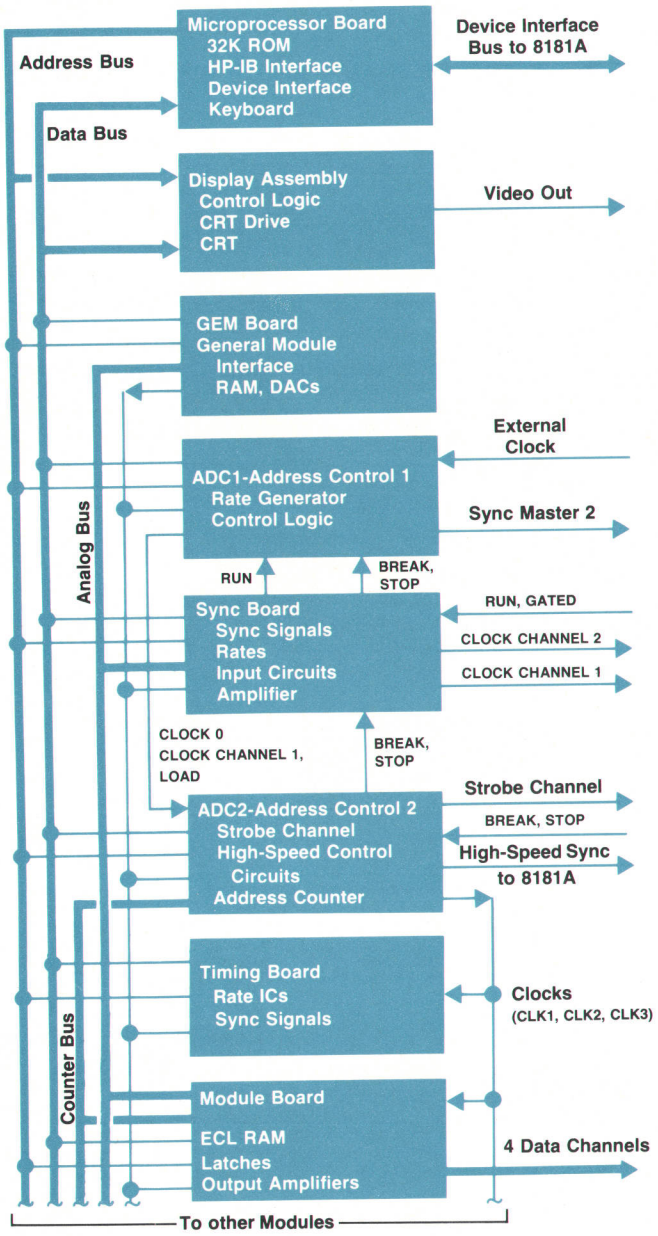

Fig. 1. *Block diagram of the 8180A Data Generator.*

- Gated cycle: a gate signal at the external **RUN** input causes data generation for as long as the input remains true. If the input goes false, the currently active cycle is completed.
- Initialization and gated cycle: operation is similar to the initialization and auto cycle mode. The currently active cycle is always completed when the gate input goes false.

In either mode, cycling ceases on receipt of a STOP signal.

Fig. 3 is a functional block diagram of ADC1. The basis of all internal timing circuits is the Rate IC. This specially developed device is used in recent HP pulse, function, and data generators.[1] Features of the Rate IC include a programmable oscillator with a range of 1 Hz to 100 MHz, programmable delay with a range of one second to 10 ns, and resolution of 100 ps or three digits when programmed by the microprocessor via a 10-bit DAC (digital-to-analog converter). Decade counters for ranging are built into the chip. The Rate IC generates the system clock in both internal and external clock modes.

Another important feature of ADC1 is the address difference counter. This 10-bit presettable counter operates continually in the count-down mode, counting clock pulses. Each clock pulse corresponds to an address. Whenever the LOAD signal goes low (Fig. 3), indicating a counter state of all zeros, the counter is preset to the difference between the first and last addresses programmed by the user. LOAD then goes high and the counter counts down until it again reaches a state of all zeros. LOAD then goes low and the cycle repeats.

A break at a defined address is performed by the strobe counter. This device is loaded by the microprocessor with the break address minus the first address.

The internal clock control generates two high-speed signals, CLK0 and CLOCK CHANNEL 1. These and the LOAD signal control and synchronize all other high-speed circuits in the 8180A and 8181A. By bypassing these signals, it is possible to set up a master-master system with two 8180As operating in parallel. In this case, only one instrument is active. The LOAD, CLK0, and CLOCK CHANNEL 1 signals are fed via a rear connector directly into the second 8180A. Bypassing is achieved automatically when the interconnecting cable is fitted.

Fig. 4 illustrates the principal signal paths on the ADC2 board. Signals CLK0, CLOCK CHANNEL 1, and LOAD are fed from ADC1 to ADC2 on twisted-pair lines by line drivers. Line receivers pick up these differentially transmitted signals, refresh them, and drive the delay lines. Another line driver generates the differential signals for the 8181A Extender. The CLK0 and LOAD signals are fed to the 8180A's address counter delayed by 10 ns to compensate for the delay introduced by the interconnecting cable to the 8181A.

The address counters support all data channels in the 8180A and 8181A. Several delay lines are required to achieve correct timing relationships with the module boards that carry the data channels (four channels per

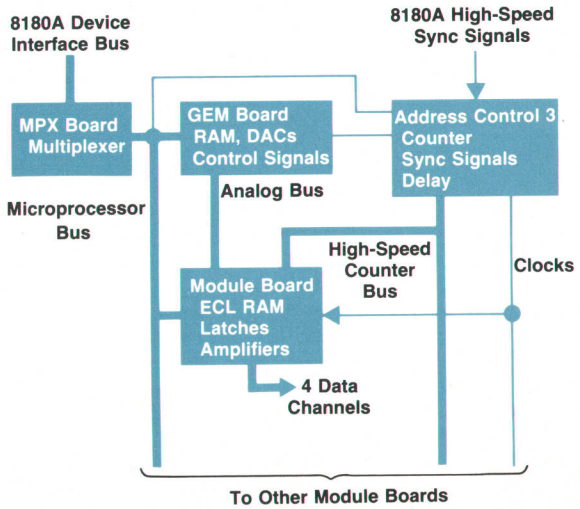

Fig. 2. *Block diagram of the 8181A Data Generator Extender.*

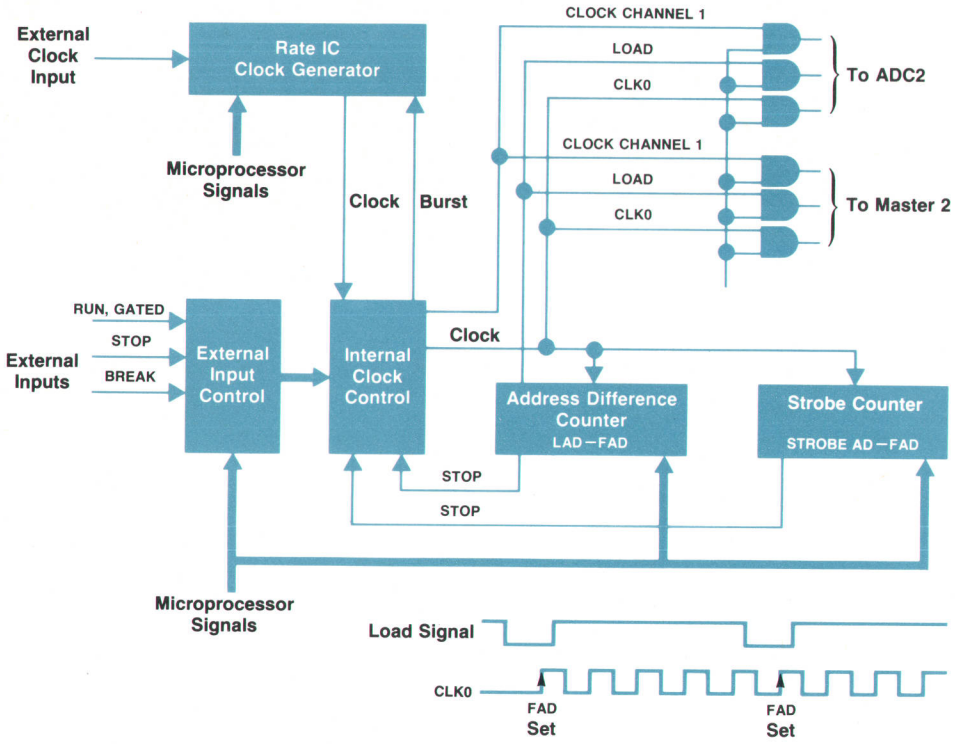

Fig. 3. *The Address Control 1 circuit generates synchronizing signals for the various 8180A operating modes.*

board). One delay line generates the signal CLK1, which guarantees sufficient setup time for the address latch. Fig. 5 shows worst-case conditions for high-speed RAM operation.

CLK2, delayed by 20 ns, latches the RAM's output data. This data then passes to the output latch after a further 10-ns delay, and finally to the XOR gate at the output amplifier input. The extra delay is necessary for generating RZ data when the instrument has been fitted with an additional timing board. Data from the data latch is fed to the reset flip-flop FF1 where, dependent upon delay and width settings, it is clocked through to the Q output. The negative-going edge resets the flip-flop in the RZ mode via the OR gate, and the XOR gate at the input to the output amplifier switches between normal and complementary operation.

In the 8181A the timing circuits on the ADC3 board are very similar to those described above. The main difference is in the programmable delay, which makes it possible to compensate for delay variations between the 8181A NRZ and 8180A data channels. The programmable delay is also needed for setting up address and data buses that differ in timing.

Timing Board

The timing board consists of four delay and width generator channels. At the heart of each channel is the Rate IC,[1] which in this application is configured to function in its timing mode. The use of conventional devices instead of Rate ICs would have taken about five times the space to achieve the same objective.

Fig. 6 shows the basic blocks of a timing channel. Inaccuracies in analog voltages generated by the DACs and peripheral components necessitate a number of control current adjustments to achieve an optimal overlap of ranges and the matching of clock inputs. The control for ranging and current programming comes from microprocessor commands sent along the bus. The function of the reset flip-flop is described in the preceding section. 32 adjustments are necessary to set up a timing board for operation, eight for each channel. Repeatability and stability results are excellent because of noncritical design and well specified components.

Module Board

The module board consists of four data channels implemented with high-speed ECL RAMs, latches for timing, and an output amplifier for each channel. With the exception of the output amplifiers, no setup or adjustments are necessary on this board. This facilitates the addition of extra boards to the 8180A or 8181A with a minimum of inconvenience. The layout of each functionally identical channel is designed in such a way that compensation for skew, introduced by the different cable lengths attached to the rear connector, is achieved by striplines on the board.

A module board complete with cables and rear connector can be fitted or replaced merely by removing two screws from the instrument's rear panel and taking off the cover. Each channel on the module board is individually screened to avoid EMI problems from neighboring channels, and to provide a heat sink for the transistors in its output amplifier.

Sync Board

The sync board consists of two clock channels, CLOCK CHANNEL 1 and CLOCK CHANNEL 2. Both channels have DACs for delay and width programming and use the same output amplifiers as the module boards. For applications that require refresh capability, CLOCK CHANNEL 1 is kept

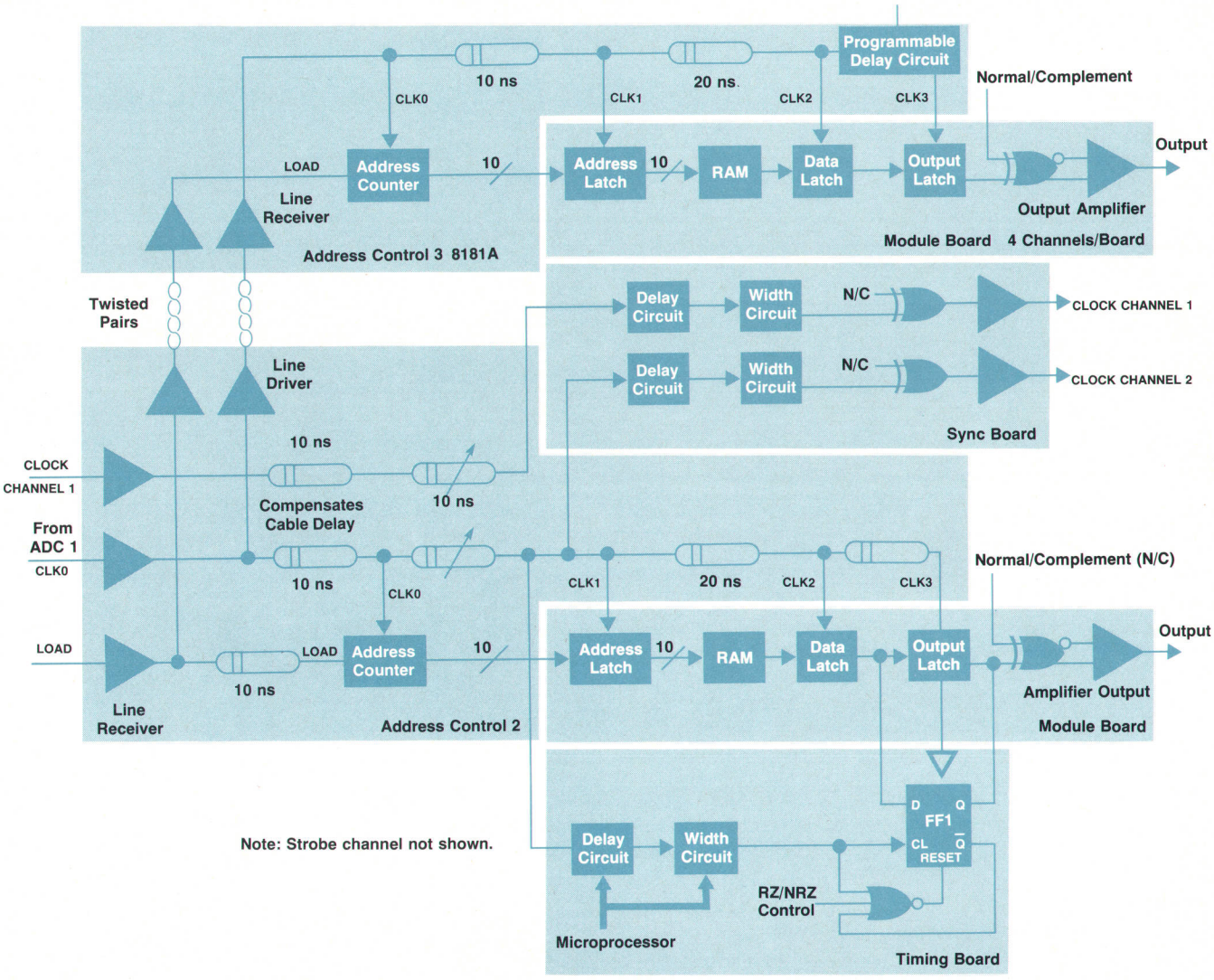

Fig. 4. *8180A/8181A timing and signal distribution.*

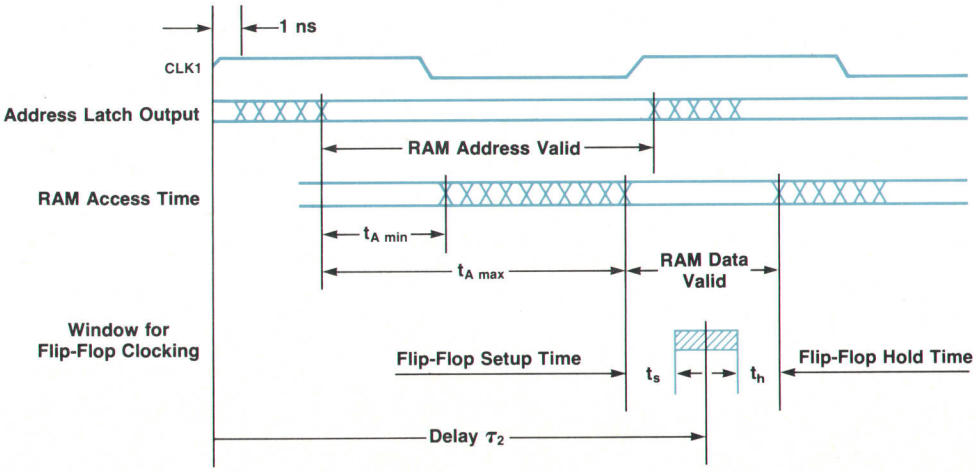

Fig. 5. *The delayed clock signal CLK1 guarantees sufficient setup time for the address latch under worst-case high-speed operating conditions.*

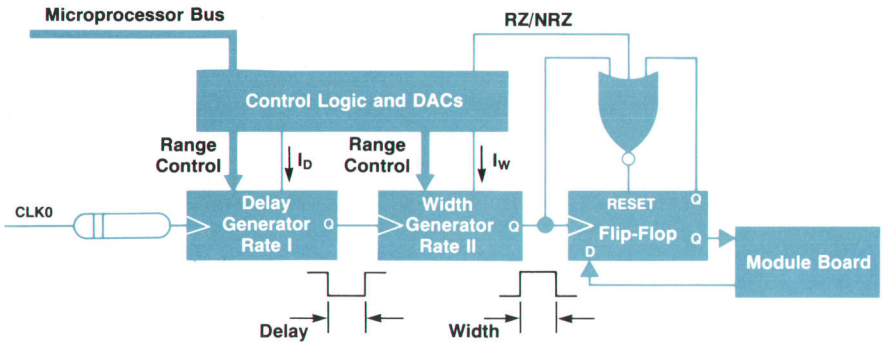

Fig. 6. *The timing board consists of four delay and width generator channels (one shown).*

running in STOP or BREAK; hence it is handled differently from CLOCK CHANNEL 2.

Output Amplifier

The final circuit in every data and clock channel is the output amplifier. It is here that timing information (high-low transitions) and dc voltages to program the high and low levels are translated into the desired pulse stream at the output. The functional diagram, Fig. 7, shows the amplifier's four major blocks. The first two form a pulse generator, and the last two a linear power amplifier.

Timing information in the form of switching commands is applied in a symmetrical ECL logic format at inputs Q and $\overline{Q}$. The signal is amplified by symmetrical complementary differential amplifiers, which control current sources in a cascade arrangement. The outputs of the four switched current generators are combined to form a pair of alternating bidirectional current sources, which drive a diode clamping bridge at nodes V_c and $\overline{V}_c$.

The clamp voltages V_c and $\overline{V}_c$ are held equal to either the upper or lower programmed voltage by unity-gain buffers U1a and U1b. In the Q=high state, the symbolic DPDT switch takes the position shown in Fig. 7. Positive current flows through D4 into the lower voltage follower U1b, and negative current through D1 into the upper voltage follower

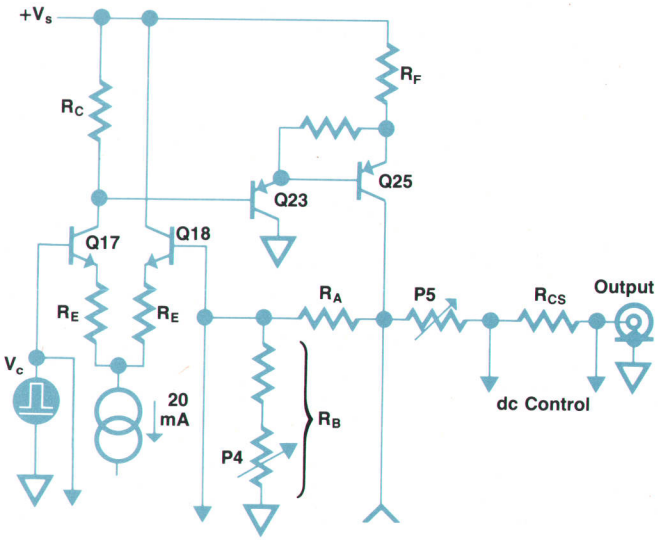

Fig. 8. *Upper branch of the linear broadband amplifier shown in Fig. 7.*

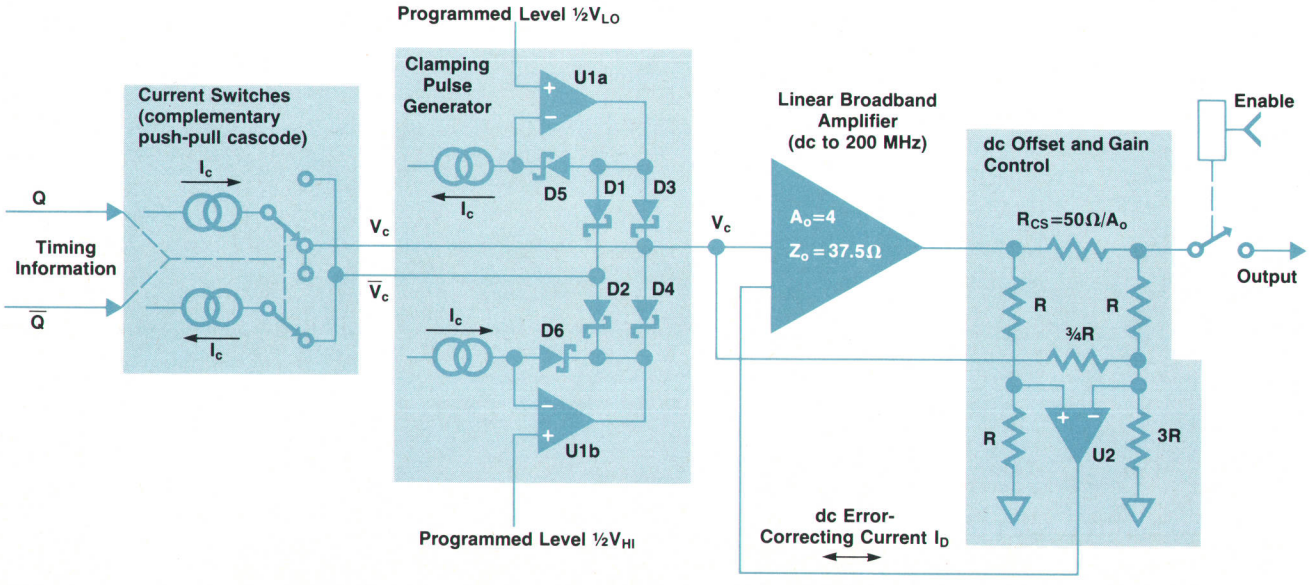

Fig. 7. *Output amplifier block diagram. The output amplifier translates timing information and dc voltages into the desired pulse stream at the output pods. The first two blocks form a pulse generator and the last two a linear power amplifier.*

U1a. As long as $V_{HI}>V_{LO}$ with at least 0.5V difference, D3 and D2 may be regarded as switched off.

Two more diodes, D5 and D6, compensate for the on voltages and temperature dependence of D3 and D4. All diodes are supplied with equal currents (I_c=15 mA). Minor differences in forward voltage drop and series resistance of the matched pairs D3, D5 and D4, D6 are corrected by trimmers. Thus V_c is equal to exactly $\frac{1}{2}V_{HI}$ when D4 is conducting (Q=high), and $\frac{1}{2}V_{LO}$ when D3 is conducting. A small error because of junction temperature differences remains in D3 and D4 when they are switched on or off. Schottky-barrier diodes are chosen for fast switching without storage delay.

The second clamping node, $\overline{V}_c$, provides a complementary pulse train to V_c. This is used for two dynamic purposes. To accelerate the high-low transitions of V_c, $\overline{V}_c$ is high-pass coupled to the bases of switched current-source transistors. The result of this additional drive is that the voltage transitions of V_c are more like pulses with constant rise time than the natural constant-slope behavior of a current-steered voltage clamp.

The second purpose of the $\overline{V}_c$ branch is to provide constant current loading for voltage-followers U1a and U1b. If D1 and D2 were not present, these op-amps would be required to deliver pulsed output currents. Frequency response limitations within the op-amps would lead to duty-cycle-dependent level variations in some critical high-frequency regions. The symmetrical clamping bridge draws dc current from U1a and U1b, keeping pulse tops flat from dc to the nanosecond region.

The clamp output signal V_c is amplified to the desired amplitude and power by a class-A push-pull amplifier. In Fig. 8, only the upper half of the amplifier, with components determining gain A_o and output impedance Z_o, is shown. The complementary symmetrical lower branch completes the amplifier for dc operation, and acts as a doubler for overall transconductance and output current. This basic arrangement is noninverting.

Minor aberrations and tolerances are trimmed out with P4, for the amplifier unloaded, and again with P5, after connection of a 50Ω load.

Output amplifiers commonly found in pulse and data generators are usually designed as current or voltage sources, both needing an internal 50Ω load to present the

Table I

Data Generator Output Amplifier Performance

Programmed load condition	from 50Ω into 50Ω (voltages double if no load connected)	from 50Ω into high impedance (≥10 kΩ)
High level range	−1.5V to +5.5V	−1.0V to +17.0V
Low level range	−2.0V to +5.0V	−2.0V to +16.0V
Resolution	3 digits (best case 10 mV)	3 digits (best case 20 mV)
Amplitude range	0.5V to 5.5V	1.0V to 17.0V
Level accuracy after	**20 ns settling time** ±0.5% of level ±3% of amplitude ±30 mV (add ±30 mV for amplitudes >0.7V)	**40 ns settling time** ±0.5% of level ±3% of amplitude ±30 mV (add ±30 mV for amplitudes >1.5V)
Level accuracy after	**1 ms settling time** ±0.5% of level ±30 mV (add ±30 mV for amplitudes <0.7V)	**1 ms settling time** ±0.5% of level ±60 mV (add ±60 mV for amplitudes <1.5V)
Transition time (10%-90%)	<3.0 ns + |amplitude| ×0.2 ns	<3.0 ns + |amplitude| ×0.5 ns
Typical transition time for ECL levels (20%-80%)	1.5 ns	--
Preshoot, Overshoot, Ringing	<±10% of amplitude	<±10% of amplitude

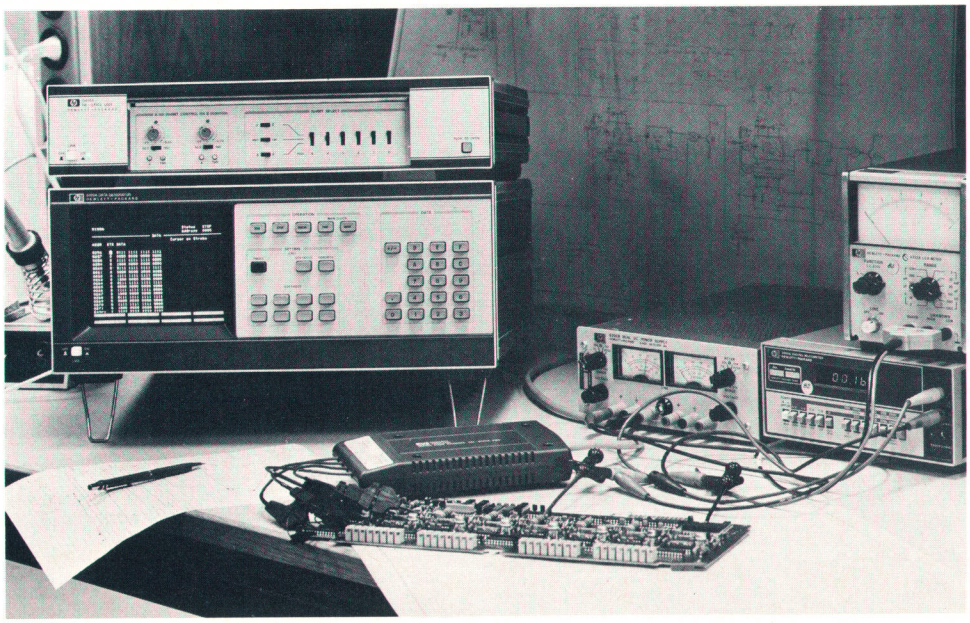

Fig. 9. *The tri-state pod makes the data generator outputs compatible with bidirectional bus and I/O pin configurations. The control and power unit on top of the 8180A Data Generator is part of the pod system.*

correct Z_o (50Ω) at their output. The amplifier concept used here gives well-defined gain and output impedance without wasting 50% of the ac power on an internal 50Ω ballast. This is important in generators in which many data channels are packed closely together, like the 8180A and 8181A.

Internal feedback in every amplifier stage (R_E,R_F) helps ensure stability and allows the use of full circuit speed (speed is ultimately limited by the propagation delay around the feedback loop in the amplifier network). The free-running amplifier produces an output signal with the specified accuracy. A dc offset of up to several hundred millivolts reflecting the thermal history of linearly operating transistors may appear, however. A dc error can also be introduced by varying the supply voltages to accommodate different output amplitude requirements. To eliminate these offsets, an additional dc control loop checks the output voltage and the output current simultaneously and ensures precise operation under any loading, level, or supply conditions.

To understand the operation of this dc control loop, look at the inputs of error amplifier U2 in Fig. 7. At the noninverting input, a voltage $V^+ = \frac{1}{2}(V_o + R_{CS}I_o)$ is compared with $V^- = \frac{1}{2}V_c + \frac{3}{8}V_o$ at the inverting input. The op-amp forces a corrective current into the inverting input of the main amplifier to keep $V^+ - V^- = 0$. The dc precision now depends on the op-amp quality and the ratio of the resistors in the voltage divider. When $V^+ - V^- = 0$, then $V_o + R_{CS}I_o = V_c + \frac{3}{4}V_o$. Since $A_o = 4$ and $R_{CS} = 50\Omega/A_o$, this expression becomes $\frac{1}{4}V_o + (50\Omega/A_o)I_o = V_c$, or $V_o = A_oV_c - (50\Omega)I_o$, which describes a linear amplifier with voltage gain A_o and an output impedance of 50Ω.

Table I shows the principal specifications of the output amplifier.

Tri-State Pod

The tri-state pod is an accessory to the 8180A Data Generator and 8181A Extender. Its function is to make the generator outputs compatible with bidirectional bus and I/O pin configurations.

The main design aims for the tri-state pod were to be able to output any level in the generator's output range of −2V to +5.5V, and to function as an analog switch, enabling the control of different logic families. At the same time, the level programmability of the system had to be maintained. Other objectives were fast switching, high output impedance with low capacitance in the off state, and low output impedance with high drive capabilities in the on state, giving high speed when driving high-capacitance loads.

The solution adopted uses the familiar diode bridge (Fig. 9). A disadvantage is that the power consumption of the bridge reduces the ratio of output to input currents significantly. This problem was solved by a complementary transistor stage that reduces the bridge supply current.

In the left-hand side of the bridge, two pairs of series diodes produce a drop of approximately 1.4V. This is always greater than the drop across the Schottky diode and

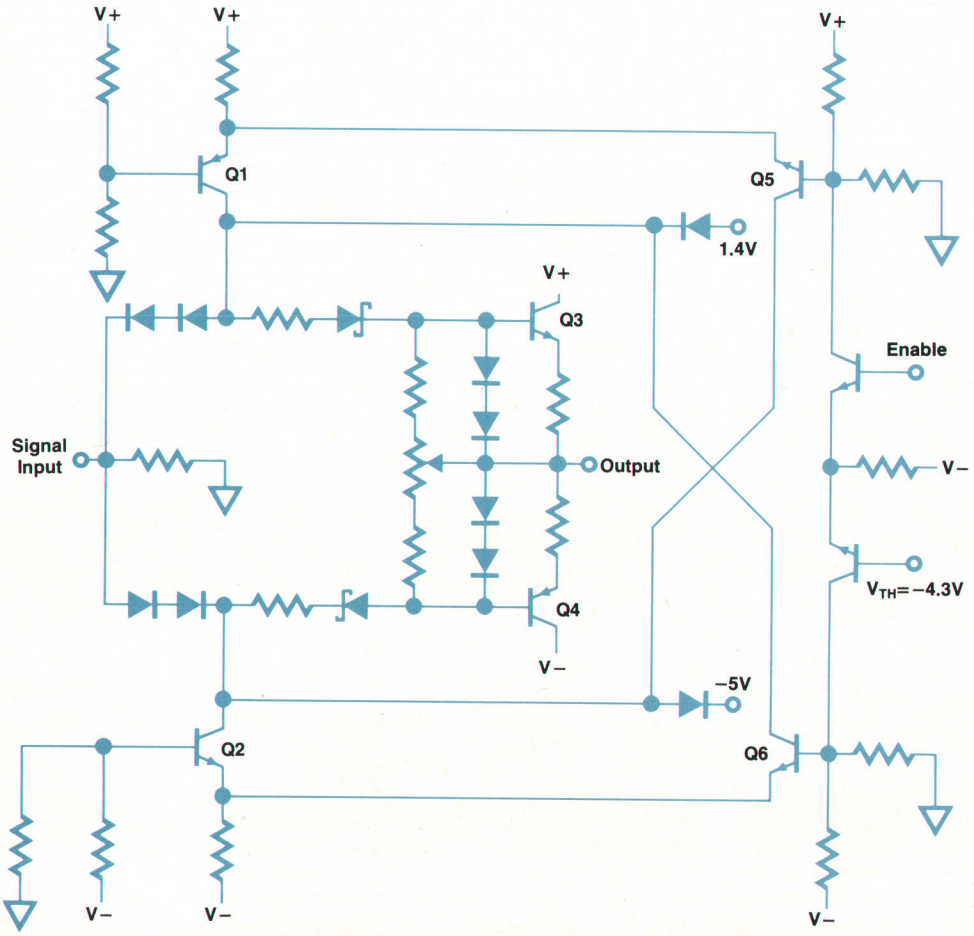

Fig. 10. *Schematic diagram of the tri-state driver.*

the emitter junction of the output transistor in each line. The series Schottky-diode-resistor configuration, in combination with an offset adjustment, permits the use of unmatched components without a reduction in level accuracy. When the enable voltage meets or rises above the −4.30V threshold, transistors Q5 and Q6 begin to conduct, thereby turning Q1 and Q2 off. In this way, the bridge becomes reverse-biased, with the clamping diodes ensuring that the output circuit is cut off when the voltage at the output is in the range −2V to +5.5V.

Reference

1. C. Hentschel, et al, "Designing Bipolar Integrated Circuits for a Pulse/Function Generator Family," Hewlett-Packard Journal, Vol. 34, no. 6, June 1983.

High-Speed Data Analyzer Tests Threshold and Timing Parameters

by Dieter Kible, Bernhard Roth, Martin Dietze, and Ulrich Schöttmer

CONVENTIONAL DATA ANALYZERS fall generally into two categories. First, there are the high-speed asynchronous timing analyzers, which produce test results similar to an oscilloscope on several channels. These analyzers are used mainly for functional analysis of random logic. Second, there are the synchronous state analyzers, which are used mostly for the functional analysis of microprocessor-based systems with real-time or other complex sequential logic. Parametric measurements, on the other hand, have to be made with oscilloscopes or timing analyzers having fairly coarse time resolution (the fastest timing analyzers available offer only 1.5 to 2 ns resolution, with a significant additional error because of skew between data channels).

The new 8182A Data Analyzer is optimized for testing threshold and timing parameters at high speeds. It has two innovative features—programmable sampling-point delay and real-time compare mode. New, specially-developed active probes with a wide range of accessories facilitate the capture of data with minimum influence on the device under test. All analog parameters, such as threshold voltages and the sampling point delay, are implemented with high resolution and accuracy. Instead of setup and hold times, a sampling time accuracy with respect to the external clock input is specified. This is more suitable for parametric measurements of integrated circuits and printed circuit boards.

The 8182A is controlled by a 6809 processor with 40K bytes of ROM space and a 14K CMOS RAM that is battery-powered for nonvolatile data storage. All I/O interfacing is memory-mapped to achieve fast access to all parameter registers.

Three Operating Modes

The 8182A has two logic analyzer modes of operation and a comparator mode. In the trigger start analyzer mode, after

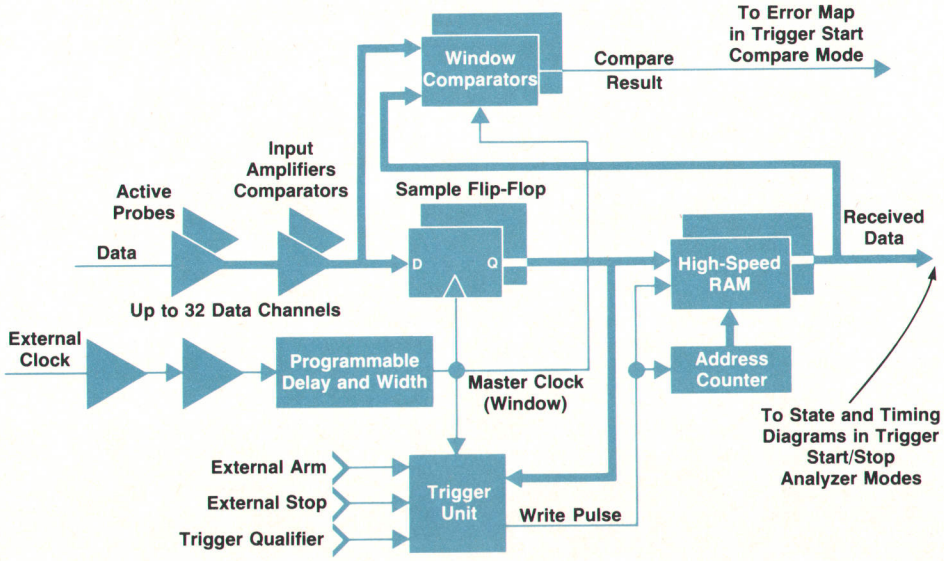

Fig. 1. *Simplified block diagram of the high-speed circuits of the 8182A Data Analyzer. New features are a programmable master clock delay and a real-time window comparison capability.*

recognizing a trigger condition, the 8182A begins to accept data into its high-speed memory. Stored data can be displayed as either state or timing diagrams, during or after completion of the measurement cycle. The microprocessor compares the received data with stored expected data and displays comparison failures on the state diagram or a concentrated overview in the error map.

In the trigger stop analyzer mode, after arming, the 8182A is always active, that is, it continually accepts data, filling and overwriting its high-speed memory. After recognition of a trigger event, it stops accepting data (after a selectable delay) and displays the previously stored data. Hence the events preceding and following the trigger event can be recorded. The monitoring capabilities are the same as in the trigger start analyzer mode.

The third mode, the trigger start compare mode, is an entirely new feature. It permits a real-time comparison of incoming data with a prestored data pattern contained in the high-speed memory. This comparison takes place during a time window synchronous with the clock input. The window is defined by a delay and a width. Every failure during the compare window generates a high logic level at a rear-panel output, and an error report can be displayed on the error map. Either one-shot or continuous cyclical measurements are possible.

Hardware Architecture

With the exception of the power supply, the display, and the microprocessor section, the 8182A hardware is to a high degree implemented with ECL to achieve 50-MHz operation and high timing accuracy. The eight-channel version of the 8182A contains two boards with digital control circuits, one board of clock generators, two boards containing the microprocessor and its interfacing, and two data boards, each with 4 channels. Six more data boards can be plugged into the remaining slots, extending the 8182A up to 32 channels. Fig. 1 shows a simplified block diagram of the hardware.

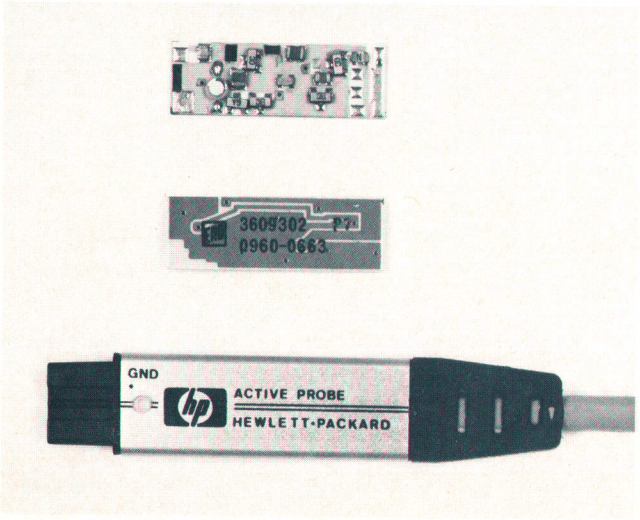

Fig. 2. *High-impedance, high-frequency, dual-threshold probing is provided by a special thick-film hybrid probe circuit.*

What Is Window Comparison?

When the 8182A Data Analyzer is in either of its logic analyzer modes, performing like a conventional analyzer, it samples a data stream on a point-by-point basis. Whatever is present between two sampling events can be analyzed with the aid of a glitch detector, but it is impossible to determine whether a glitch appeared at the beginning or end of a sampling period. Similarly, determining the stability of a logic level during any part of the sampling period is also a problem.

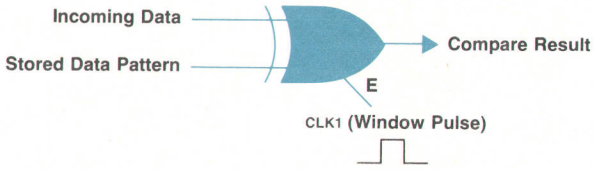

Fig. 1. *In comparator mode, the 8182A Data Analyzer compares incoming data with stored data during a time window of programmable width.*

How can the status of data on a microprocessor bus be determined during the period beginning 50 ns before and ending 10 ns after a clock edge?

When the 8182A is operating in its comparator mode, a periodic time window can be programmed. During this time, the incoming data can be compared with an internally stored pattern. The time window is synchronous with the clock connected to the 8182A clock probe.

The comparison circuit consists of an XOR gate in each channel, which compares the incoming data with a fixed data pattern. A pulse of the desired window width (60 ns in the example given here) is applied to the enable input of the gate (see Fig. 1).

Fig. 2 shows the gate output. It is assumed that the stored data pattern consists of low levels, so an incoming high generates a positive pulse at the gate output while the window pulse is high. In Fig. 2a and 2b a failure is recognized. Fig. 2c and 2d are borderline. The compare error may not be recognized, although one

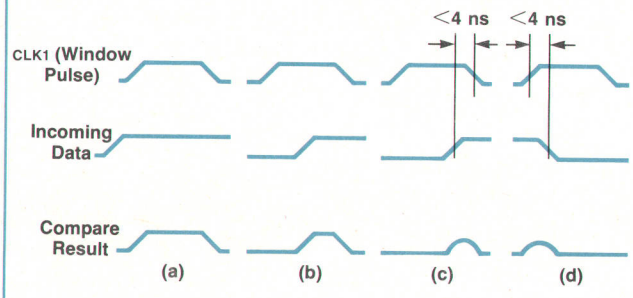

Fig. 2. *Assuming that the stored data pattern consists of all low levels, an incoming high level during the window causes a positive compare result. Failures (a) and (b) are easily recognized, while cases (c) and (d) are borderline.*

edge of the incoming data lies within the time window. At the 8182A input, the incoming data edge must be within 4 ns of the window edge for an error to be diagnosed correctly.

-Martin Dietze

Active Probes and Input Amplifiers

To achieve the design goals of high-impedance, low-capacitance probing with high-frequency and dual-threshold capabilities, a special active probe circuit was developed. It is realized as a thick-film hybrid circuit (Fig. 2).

The dimensions of the hybrid are 29.7 mm × 10 mm × 2.4 mm. Special care had to be taken in designing the high-impedance input stage layout to achieve the small input capacitance of less than 7 pF (the hybrid alone has only a 4.5-pF input capacitance). The hybrid is packaged in a small aluminum case and connected to a special 1.5-m cable consisting of two shielded cables, one of which is 50Ω coax, and two single wires for power and compensation for ground potential differences. Four of these active probes and cables share a single connector, which can be connected to the rear panel of the instrument.

Fig. 3 is a diagram of the active probe and input amplifier circuit. At the probe input, a spark gap (a laser-cut thick-film resistor) limits electrostatic discharge to several hundred volts. The input information V_{IN} is divided into an ac path and a dc path. The ac signal is FET-buffered after frequency-compensated voltage division by 5 and sent to the analyzer by a line driver with a series termination. At the analyzer end of the cable, the signal is inverted.

The dc path is a simple op-amp circuit with a gain of −0.2. The input signal is level-shifted according to the threshold voltage so the high-speed comparator always compares its input signal with zero volts. Since the dc input is brought to the instrument at virtual ground, the input characteristics of the active probe remain constant with frequency. The capacitance of the line has no influence, and cable noise is significantly reduced.

After the incoming signal has been divided by 5 and shifted according to the programmed threshold, it is applied to a high-speed comparator, which has a few millivolts of hysteresis to suppress noise and high-frequency oscillation.

The 8182A is capable of comparing the incoming data with two thresholds simultaneously. For this, two neighboring channels are combined by relays in the following manner. The threshold comparator of one channel is disconnected from its input amplifier and connected to the amplifier of the other channel, so that the second channel sends its signal to two comparators. The first channel is then switched off. One comparator is used to compare the low-level threshold and the other to compare the high-level threshold. The data from both comparators is stored in two memory channels before the microprocessor combines them into one report. Eight channels can always be selected to perform dual-threshold measurements on four data inputs.

Data Sampling in the Logic Analyzer Modes

In the trigger start analyzer mode and the trigger stop analyzer mode, the data being digitized by the comparators is sampled in the sample flip-flop by the master clock (Fig. 1). The sample flip-flop is the heart of the analyzer. It has excellent sampling jitter characteristics (50 ps or less) and low temperature drift. The sampling jitter of a D-type flip-flop is the time interval between the specified setup and hold times where the output is not defined.

Variable delay lines in the data channels are used to compensate for the clock circuit's propagation delay and the sampling flip-flop's setup and hold times (more about this later).

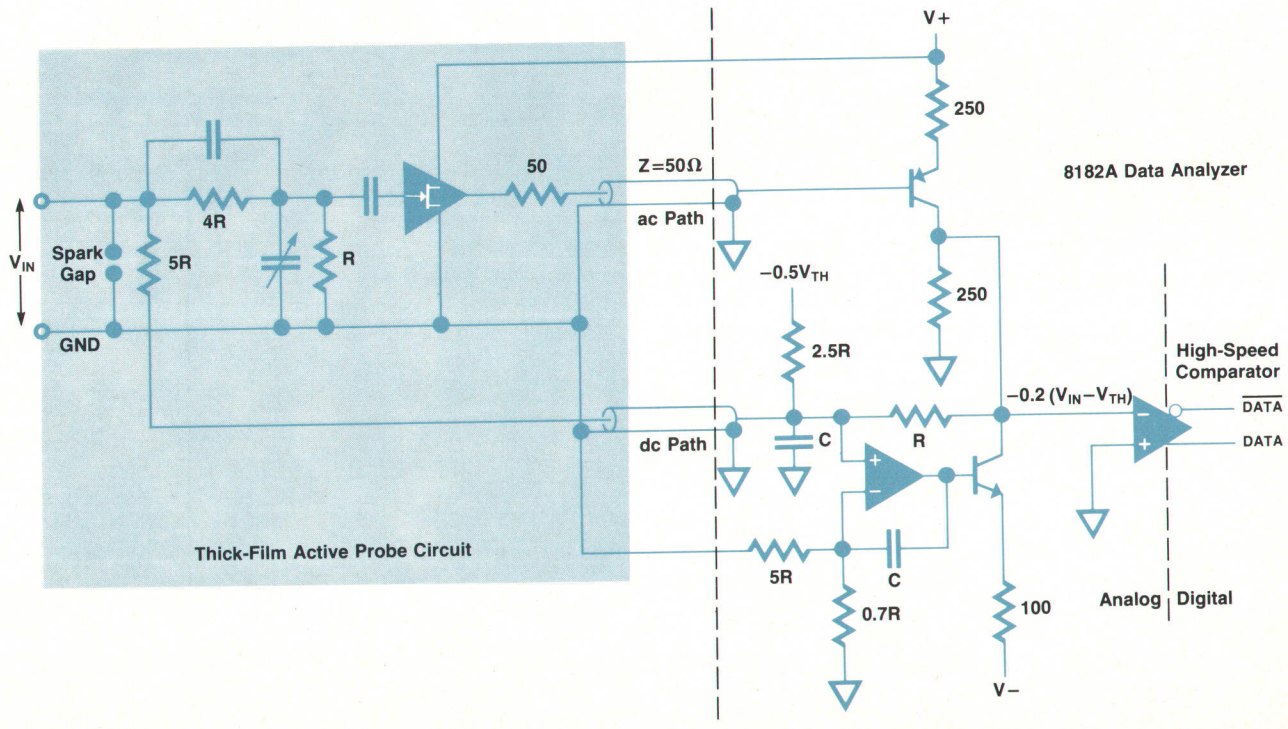

Fig. 3. *Active probe circuit and analyzer input amplifier circuit.*

The sampled data is written into the high-speed RAM by the gated write pulse generated by the trigger unit. The data can also be compared by the microprocessor with a fixed data pattern contained in the reference memory. A previously received data pattern contained in the high-speed RAM can be dumped into the reference memory. The reference memory can also be loaded and modified via the keyboard.

Interactive Read

A novel feature of the trigger start analyzer mode is the interactive read circuit. It permits the microprocessor to read the contents of the high-speed RAM cells during data sampling without losing data. This means that at a slow clock rate, the sampled data can be displayed immediately on the screen (e.g., on the timing diagram) after every sample. Therefore, it is unnecessary to wait until a measurement has been completed before seeing the result on the screen, unlike almost all other logic analyzers.

A special circuit to perform the difficult task of timing the interaction of the microprocessor and the asynchronous sampling was developed. A simplified diagram is shown in Fig. 4. A READ/$\overline{\text{STORE}}$ signal is generated from the master clock by a retriggerable monostable multivibrator (one-shot) and applied to an address multiplexer. For 50 ns after each positive transition of the master clock, the outputs of the high-speed address counter are tied to the RAM address inputs and a sampled word is stored. The multiplexer then applies the microprocessor-controlled read address to the RAM address inputs. If a read request ($\overline{\text{RDRQ}}$) was initiated by the microprocessor, the circuit now starts reading the RAM contents at the read address. $\overline{\text{RDRQ}}$ is stored in FF1.

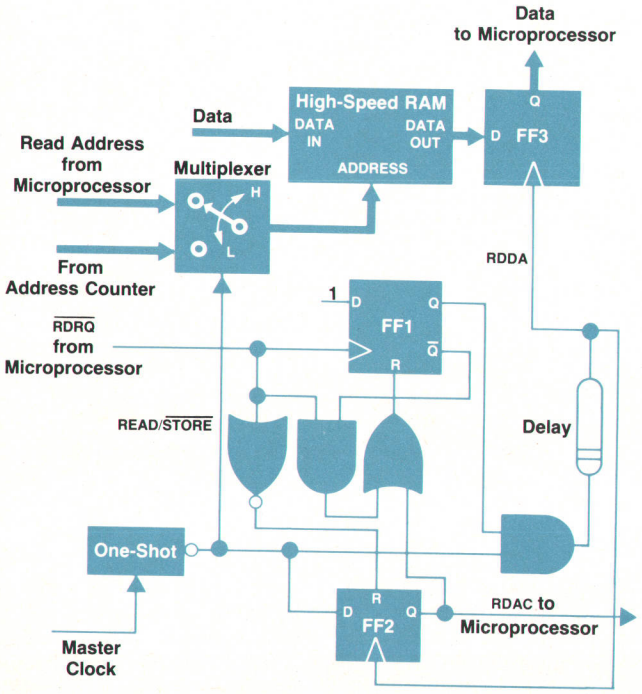

Fig. 4. *The interactive read circuit lets the microprocessor read the contents of the high-speed RAM during data sampling without losing data.*

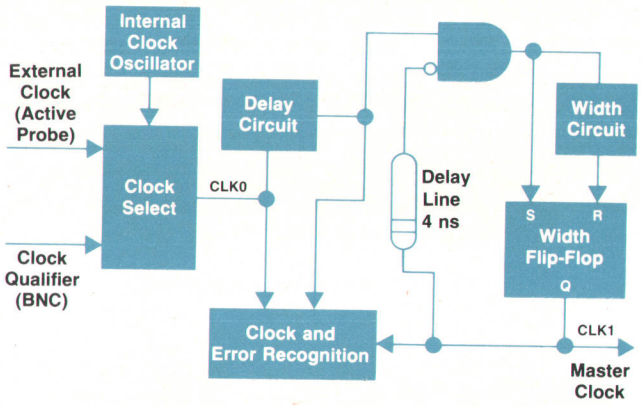

Fig. 5. *Clock timing circuits produce the programmable delay and the programmable width of the master clock.*

The ANDing of the Q output of FF1 and READ/$\overline{\text{STORE}}$ generates a read data (RDDA) signal, storing the contents of the chosen RAM cell in FF3 after an appropriate delay (RAM access time). If this read activity is not interrupted by the next master clock, RDDA generates a read acknowledge (RDAC) signal, which informs the microprocessor that valid data has been stored in FF3, and FF1 is reset. Now the microprocessor can read the content of FF3 and initiate another read request.

If the read process has been interrupted by a new master clock, which has a higher priority, the multiplexer switches immediately to the address counter. Sampled data is then written into the RAM. Meanwhile, the RDDA signal is terminated and RDAC is suppressed. After the one-shot's period has elapsed, the signal RDDA is reinitiated. This process is repeated until the RAM has been successfully read.

Real-Time Comparison

In the trigger start compare mode, the high-speed RAM is used to read out expected data in real time for comparison with incoming data. The same patterns are used in both logic analyzer and comparator modes. The high-speed RAM contents and the data from the active probes are sent simultaneously to the window comparators (see Fig. 1). There they are compared channel by channel during a time interval determined by the delay and width of the master clock. The compare results of all channels are then ORed. The output of the OR gate is qualified with a status signal and the word mask signal (discussed later). The result is immediately available at the rear-panel **PULSED ERROR** output. The result of every word comparison is stored in a special RAM that has one bit for each address. The contents of this RAM form the error map.

A second error output, **LATCHED ERROR**, is driven by a flip-flop that is set by the first error during a comparison sequence. This output remains high after the end of the measurement for further processing. It is reset when a new measurement is started. A character string in the display labeled Compare Failed/Passed shows the status of the latched error output.

Channels that have failed are marked on the displayed error page. To obtain this information, the output of every

channel's window comparator is processed separately. The result of any real-time comparison is two-dimensional, with both faulty words (Y) and faulty channels (X) identified. To analyze any failures that are discovered, the logic analyzer modes can be used.

Sometimes there is no requirement to compare the results of all channels or all words. The 8182A is equipped with a means for disabling individual channels and inhibiting the compare results for individual words by setting them to "don't care." Individual words are inhibited by a separate word mask memory, running in parallel with the high-speed RAM. Its output is gated with the real-time compare result.

Clock Timing

Clock timing circuits on the clock board produce the programmable delay and the programmable width of the master clock. A simplified diagram is shown in Fig. 5. The active clock CLK0 is a combination of the external or internal clock and the clock qualifier input.

The internal clock is generated by a 100-MHz oscillator, divided down in 1-2-5 steps. CLK0 triggers the delay circuit, which sets the width flip-flop, which is reset by the width circuit. The flip-flop output is the master clock, CLK1.

Delay and width generation is done mainly with custom ICs, as it is in the 8180A Data Generator (see Fig. 6). However, in the analyzer, it is of great importance to keep the

Generation of Analog Voltages

A multichannel instrument with universal features, working with several logic families, requires the ability to attach various programmable thresholds to different probes. In addition, features like delay and width, also programmed by analog voltages, are required. Therefore, many programmable voltages had to be made available in the 8182A Data Analyzer. The actual number is 42. These voltages are generated cyclically by a single digital-to-analog converter (DAC) and sent serially to all the places where they are required. On arrival, sample-and-hold circuits select the desired level at the desired time (see Fig. 1).

Addresses and logic control signals are generated by the counter. The RAM, which stores 11-bit words to be used in level generation, delivers information to the DAC for conversion. The dc levels are then passed to the sample-and-hold circuits, together with logic control signals and address information. Fig. 2 shows a simplified sample-and-hold circuit. Amplifier 1 charges the capacitor during the time that the enable signal is low, and amplifier 2 tracks that voltage. The feedback in the circuit eliminates the offset voltage of amplifier 2.

-Bernhard Roth

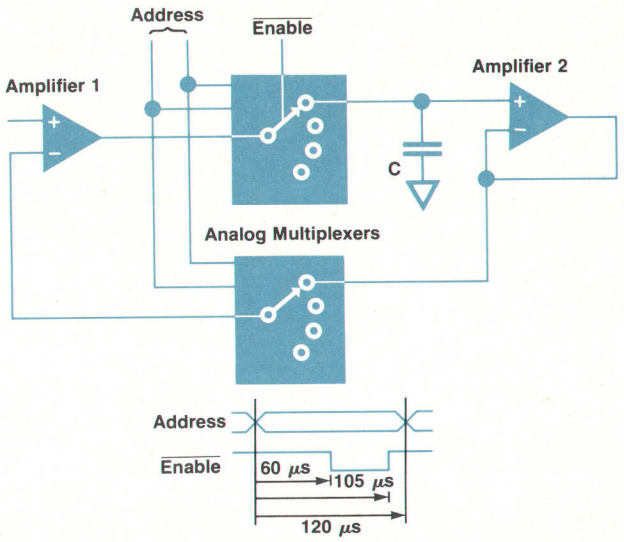

Fig. 2. *Sample-and-hold circuits at various points in the analyzer select the correct analog voltage at the correct time.*

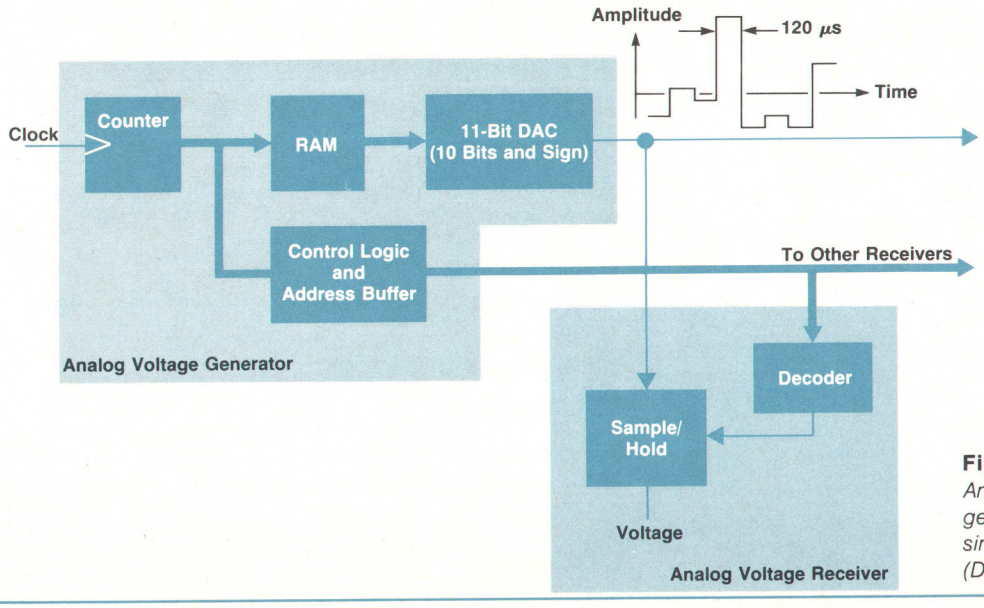

Fig. 1. *In the 8182A Data Analyzer, 42 analog voltages are generated by time-multiplexing a single digital-to-analog converter (DAC).*

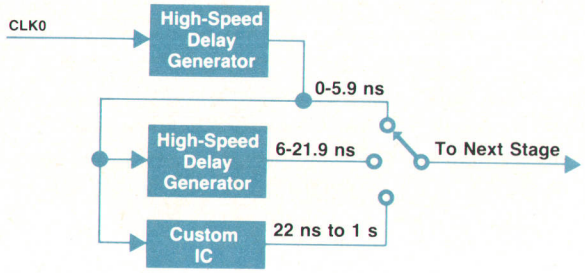

Fig. 6. *Custom ICs are used in the delay circuit (shown) and the similar width circuit. Special high-speed delay generators minimize the delay through the circuit.*

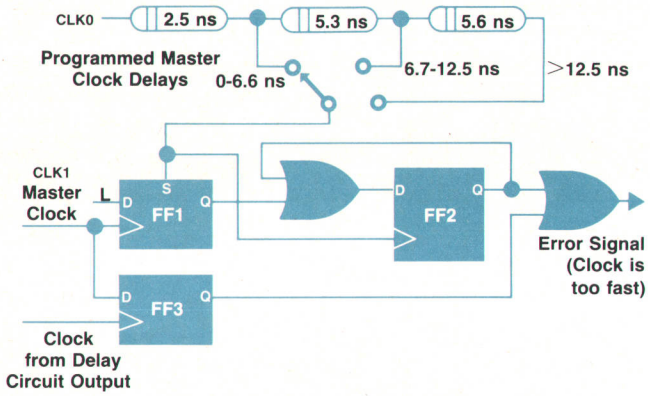

Fig. 8. *An error recognition circuit signals the operator when the time between two consecutive active clock pulses is too short to produce two correct master clock pulses.*

fixed delay through the circuit to a minimum. The reason for this is that every data channel also has to be delayed to achieve the specified sampling accuracy. For this reason, special high-speed delay generators implemented with 100k ECL are used. These have a minimum fixed delay and a variation of up to 20 ns. A simplified circuit diagram is shown in Fig. 7.

An incoming edge sets the flip-flop. Output Q opens the switch, forcing current I to charge capacitor C, creating a positive-going ramp. I is generated from the signal U by an analog divider. The instant the threshold voltage is reached, the flip-flop is reset and C is discharged. The pulse width at the output of the comparator is determined by the propagation delay through the components. The fixed delay is roughly 6 ns and the variable delay is proportional to U. Current I_1 is used to improve linearity.

Since the main application of the data analyzer is in synchronous operation with programmed delay and/or width, constant observation of the external clock in relation to the actual delay and width is necessary to ensure that every active input clock edge creates a correct master clock pulse. When the time between two consecutive CLK0 pulses is too short to produce two correct master clock pulses, the operator is informed. This task is accomplished by an error recognition circuit (see Fig. 8).

Error recognition is performed along two paths. The first is FF1/FF2, and the second is FF3. The delayed CLK0 sets FF1 and samples FF1's output with FF2. The master clock resets FF1, so that the whole process starts again. If two CLK0 pulses occur before a master clock edge, the second CLK0 pulse causes FF2's output to go high and hold that status. The delay circuit output samples the master clock with FF3. FF3's output goes high if the width circuit (see Fig. 5) is triggered too fast. If one of the paths recognizes that the clock is too fast, the corresponding message appears on the display and all flip-flops are reset by the microprocessor, which then continues to poll the error circuit.

The master clock is buffered and sent on five transmission lines of equal length from the motherboard to all data channels and control circuits.

Trigger Unit

Triggering of the 8182A depends upon a combination of the states of the trigger arm input and the trigger qualifier, the appearance of the trigger word at the data inputs, and the state of the trigger event counter.

When the **RUN** key is pressed, the 8182A goes into the armed state and begins to search for trigger events. The trigger arm input is edge-triggered and serves as a preset input. The trigger qualifier and trigger word must be true at the same time to clock the trigger event counter, which runs in two modes:

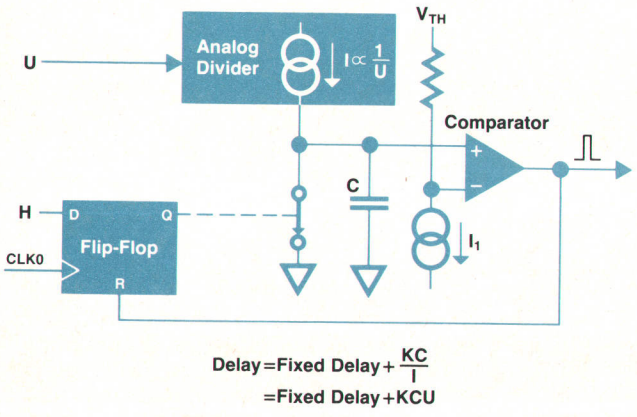

Fig. 7. *Simplified circuit diagram of the high-speed delay generator.*

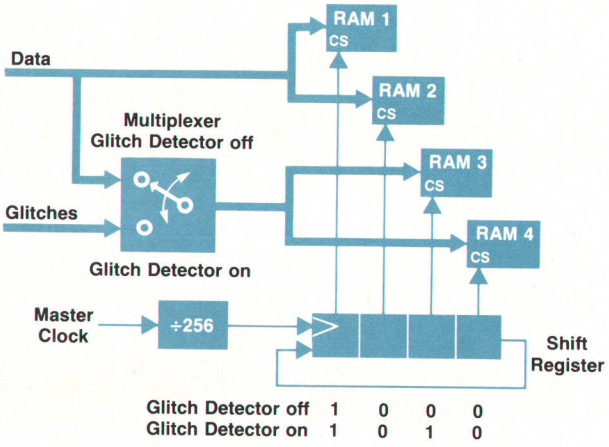

Fig. 9. *For glitch detection, the high-speed RAM is split into data and glitch memories of equal size.*

1. "Allow gaps yes." After the programmed number of true trigger events has been counted, the trigger event counter activates the trigger delay counter.
2. "Allow gaps no." Only true trigger events that occur one after the other at every master clock time are counted. If a false trigger event is recognized, the counter is reset to zero.

When all trigger conditions are true, the trigger delay counter, which consists of a count-down circuit that can be preset to any value between 0 and 65535, is started. When the delay counter has reached zero, the 8182A responds to the trigger condition. In the trigger start analyzer mode, it begins to write the incoming data into the high-speed RAM. In the trigger stop analyzer mode, it stops data recording. In the trigger start compare mode, it begins the comparison of incoming data.

All trigger conditions can be set to "don't care," that is, they appear to be always true. The 8182A then starts immediately with the first incoming active clock edge. The instrument can also be started immediately by pressing the **SAMPLE** key, which overrides all trigger conditions and generates one clock pulse. Pressing the **SAMPLE** key repeatedly or holding it down generates additional clock pulses for storing or comparing data manually.

Glitch Detectors

Each channel of the 8182A has its own glitch detector. In contrast to the latch mode found in many analyzers, the glitch detector allows the 8182A to differentiate between a data transition and a glitch, which is defined as more than one data transition per sampling interval. To store the detected glitches in addition to the sampled data, the high-

Testing the Key Specifications of the 8182A

Since the 8182A is an analyzer, and key specifications such as sampling accuracy (±1 ns) and threshold accuracy (±10 mV) refer to inputs, direct measurement of these important values is extremely difficult. Instead, signals must be applied and conclusions drawn about the performance of the instrument from its response.

Fig. 1 illustrates a method by which it is possible to measure the actual sampling point and threshold directly. The heart of this test system is an electronic tool consisting of a simple integrating op-amp circuit and a voltage-controlled delay generator. The 8182A can be programmed and configured to appear as a voltage comparator followed by a D-type flip-flop. For this application, the 8182A can be considered as a level comparator for the data inputs, and as a phase comparator for data inputs with reference to the clock input.

The closed loop consisting of the 8182A, integrator, and voltage-controlled delay generator provides a data slope at the active probe's input at the precise time of the actual sampling point. The measurement of the sampling point can now be performed simply by a time interval counter.

The threshold measurement is performed using the closed loop without the delay generator, thus passing the output of the integrator to the data inputs. The resulting voltage level is read with a DVM.

-Bernhard Roth

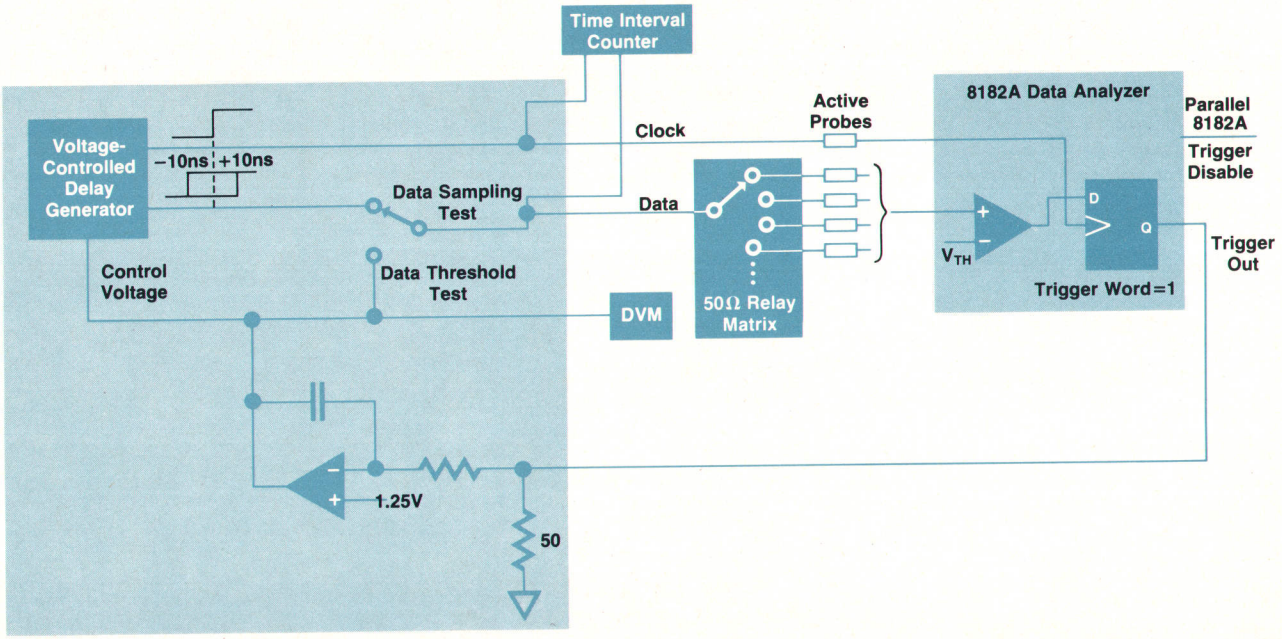

Fig. 1. *An integrator and a voltage-controlled delay generator make it possible to measure the 8182A Data Analyzer's sampling point and threshold directly.*

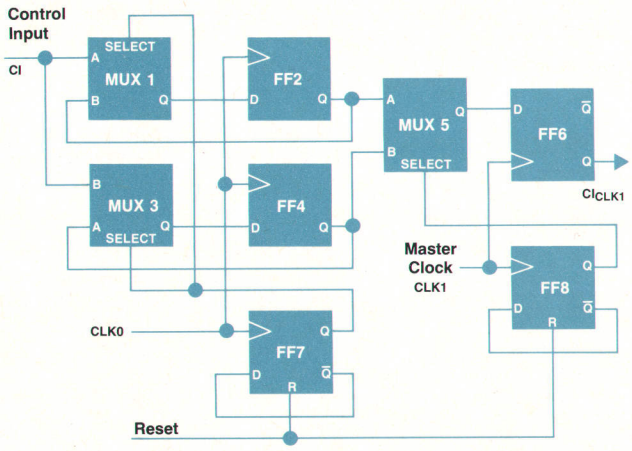

Fig. 10. *This correlator circuit attaches the trigger control input sampled by CLK0 to the appropriate master clock (CLK1) pulse. Thus it prevents erroneous triggering resulting from the variable sampling point delay.*

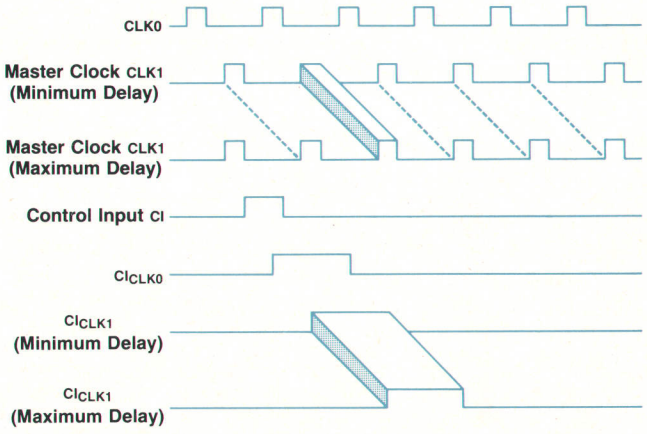

Fig. 11. *Timing diagram for the correlator circuit of Fig. 10.*

speed RAM is divided into data memory and glitch memory, each having a capacity of 512 bits per channel. Therefore, when the glitch detector is switched on, the memory capacity of each channel is halved.

Fig. 9 shows the organization of the high-speed RAM. Each channel stores its data in four 256 × 1-bit RAM arrays. The CS signals are provided by a shift register. When glitch detection is off, data is simultaneously switched by the multiplexer to each of the four RAM fields. The shift register is preloaded with (1,0,0,0). After 256 master clocks, the contents of the shift register are advanced one cell to the right, resulting in (0,1,0,0). In this way, all four RAM arrays are enabled in sequence and filled with data. When glitch detection is on, the multiplexer separates the RAM inputs so that data goes to RAM arrays 1 and 2, and glitches to arrays 3 and 4. The shift register is then preloaded with (1,0,1,0). Thus, arrays 1 and 3 are enabled at the same time, with 2 and 4 following 256 clock pulses later.

The glitch detector used in the 8182A is a modified version of the well proven detector in the 1615A Logic Analyzer,[1] improved to perform at 50 MHz. In principle, the glitch detector consists of a pair of edge-triggered flip-flops (one for positive edges and one for negative edges) that

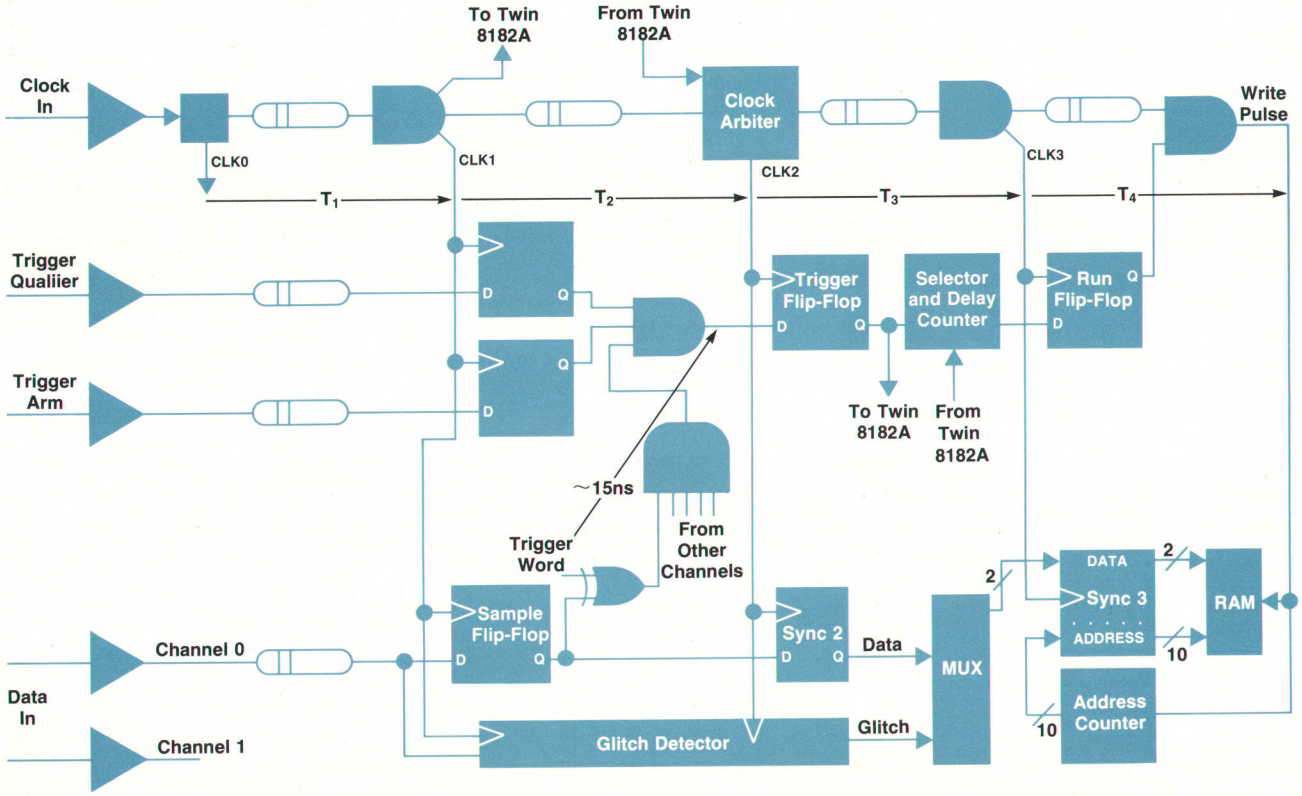

Fig. 12. *Block diagram in logic analyzer modes. A multiphase clock system and data pipelining are used.*

serve as pulse stretchers, lengthening every glitch so that it can be sampled by the master clock. To avoid dead times during resetting of the glitch detectors, each edge-triggered flip-flop is duplicated. While one pair of flip-flops is active to receive a glitch, the other is reset after its glitch information has been written into the glitch memory. Obviously, very careful design of the circuit and printed circuit board was necessary to achieve accurate 50-MHz operation.

Control Input Correlators

A special problem arose because of the programmable sampling point delay. With an increase in the sampling point delay, the relationship between the master clock and the initial CLK0 is modified, and this can result in erroneous triggering. To avoid this phenomenon, the sampling of the control inputs (clock qualifier, trigger arm, trigger qualifier, and external stop) is performed with the undelayed signal CLK0. This gives an exact specification of the control input's sampling point delay.

A correlator circuit (Fig. 10), has the task of attaching the control input sampled by CLK0 to the appropriate master clock (CLK1) pulse. This task could have been performed by programmable delay lines, but the 8182A uses a simpler way, a digital circuit that adapts automatically to different delay settings.

The key idea is to store the sampling result of clock phase CLK0 in two input registers for two clock periods, each with one clock period offset.

The output register takes the appropriate information from the input registers via a multiplexer, which is clocked by the delayed clock phase CLK1. The whole process is controlled by flip-flops FF7 and FF8, which have to be initialized correctly to maintain the phase relationships.

The minimum propagation delay time between CLK0 and CLK1 is 10 ns (with CLK1 programmed to 0 ns added delay), which is equal to the maximum allowable propagation delay for FF2 and multiplexer MUX5 and the setup time of FF6. If the CLK1 delay is increased to more than one clock period, no problem arises.

Fig. 11 is a timing diagram for the correlator circuit, Fig. 10.

Time Relationships in the Logic Analyzer Modes

In the logic analyzer modes (i.e., trigger start analyzer and trigger stop analyzer modes), a multiphase clock system and data pipelining are used (see Fig. 12). The clock phases are derived from CLK0 via delay lines. The multiphase system makes it possible to sample, trigger, and store data on the same clock pulse. Data is sampled on transitions of the master clock CLK1, which can be delayed relative to the clock input. The sampled data is captured by SYNC2. The trigger word is detected simultaneously and stored by the trigger flip-flop at clock phase CLK2. The trigger information is fed through a selector to the run flip-flop. Data and memory addresses are sampled by CLK3. With the run flip-flop active, write pulses are supplied and data is written into the high-speed RAM. Memory addresses are supplied by the address counter, which is incremented by the write

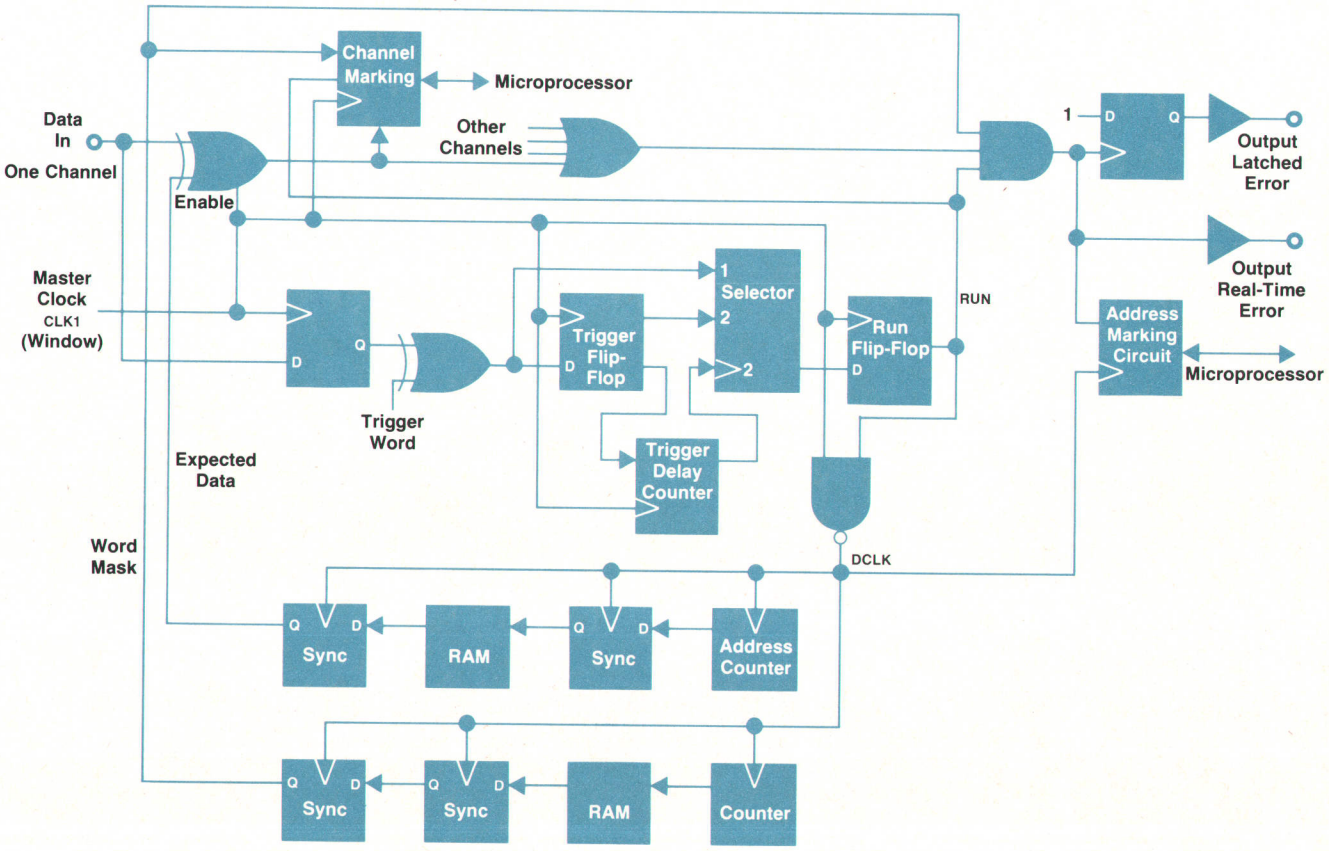

Fig. 13. *Block diagram in comparator mode.*

pulses.

Since the maximum sampling rate is 50 MHz (20 ns period), the clock phases must be within 20 ns of each other to achieve synchronous operation. On the other hand, the propagation delay of the trigger word is roughly 15 ns because of some gating operations and the motherboard connections. In the twin or parallel operating mode, trigger information sent to and received from the second 8182A via a twisted-pair cable takes about 12 ns excluding gate propagation delays. With these values in mind, the timing of clock phases CLK1 to CLK2 and CLK2 to CLK3 becomes rather critical. Therefore, delay times T2 and T3 are adjusted individually to 18 ns. To allow for the data and address setup time specifications and the write pulse width delay of the high-speed RAM, T4 is set at 7 ns and the write pulse width is 7 ns.

Timing in the Comparator Mode

The timing system for the comparator mode (i.e., the trigger start compare mode) is somewhat different from the logic analyzer modes because data is not sampled and written into memory. Instead, incoming data is compared in real time with data read from the high-speed memory. The compare result cannot be pipelined because of its analog character. Unfortunately, trigger word detection and processing takes time, as it does in the logic analyzer modes. To avoid a trigger delay that is a function of frequency, the clock inputs of the trigger and run flip-flops are modified to be synchronous with clock phase CLK1. This results in a fixed minimum trigger delay of 1 clock period. In twin operation, the minimum trigger delay is increased to two clock periods.

Fig. 13 is a block diagram of the instrument in comparator mode. After the run flip-flop is triggered, a clock pulse

Interfacing the Device Under Test

Multichannel instruments with high-frequency capabilities such as the 8180A Data Generator and the 8182A Data Analyzer require special attention to the problem of DUT interfacing.

The design goals were easy adaptability, good signal performance, universal interface capabilities, and suitability for all generator and analyzer requirements.

A special connector is located at the front end of the analyzer active probe (see Fig. 1a). At the generator end, the same connector type is molded directly onto a 50Ω coaxial cable (Fig. 1b). Six accessories for various interface possibilities were designed:

- Grabber with ground lead (Fig. 1c)
- BNC adapter (Fig. 1d)
- SMB adapter (Fig. 1e)
- Adapter for the HP 10024A IC Test Clip (Fig. 1f)
- Open-ended adapter for a custom connector or fixed wiring (Fig. 1g)
- Solder-in receptacles for printed-circuit boards (Fig. 1h).

-Horst Link

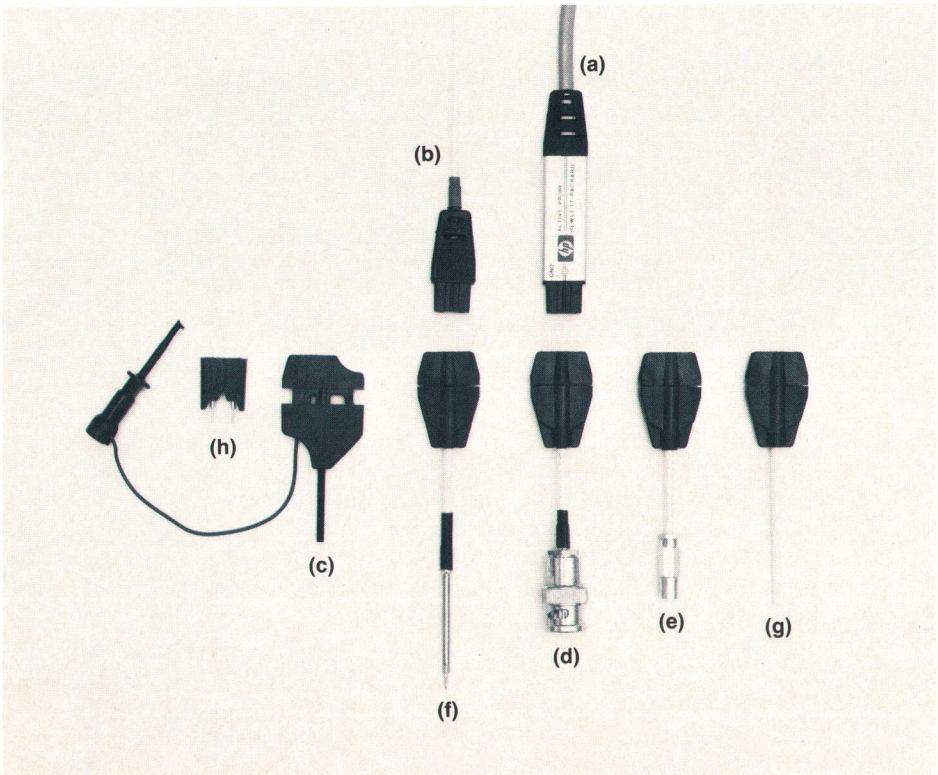

Fig. 1. *8182A Data Analyzer active probe and accessories.*

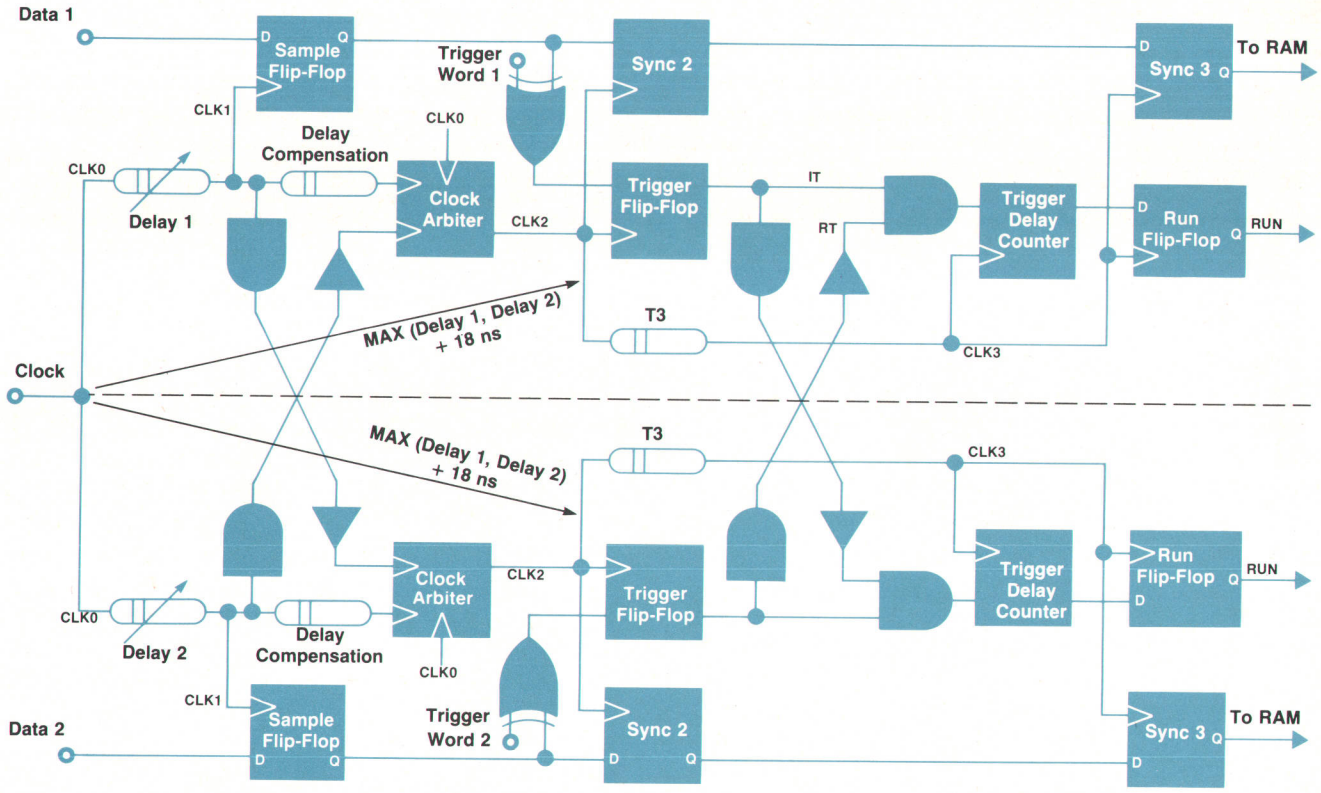

Fig. 14. *In parallel or twin operation of two 8182A Data Analyzers, clock arbiter circuits synchronize the two units in the logic analyzer modes. In comparator mode, the arbiters are not used.*

(DCLK) is generated at the end of the time window signal (CLK1). This prepares the next data word for comparison, supplies the next address to the RAM, and increments the address counter and the word masking circuit, which provides for the masking of errors at every user-selectable address. The compare result of every word is stored by the address marking circuit. The channel marking circuit pinpoints the channel or channels in which a compare failure has occurred. Interrogation of the address marking and channel marking circuits gives the microprocessor the information required to generate the error map.

Parallel Operation

The 8182A is designed to run with another 8182A in parallel. This configuration increases the number of channels up to maximum of 64. For this purpose, both instruments are tied together with a multiple-conductor cable which synchronizes the trigger conditions. The clock probes of both instruments are connected to the same external clock source to maintain high sampling accuracy and low skew.

The user must ensure that both instruments are programmed compatibly. Parameters such as trigger conditions, sampling point delay, and thresholds are individually programmable for both instruments. The trigger delay counters of both instruments can be programmed independently. Hence the start of one 8182A can be delayed with respect to the other for a defined number of clock periods.

The clock arbiter synchronizes clock phases CLK2 and CLK3 of both 8182As in the logic analyzer modes. The arbiter output pulse (CLK2) is delayed by 18 ns with respect to whichever CLK1 has the greatest delay (see Fig. 14). Basically, the circuit consists of two high-speed 100k ECL D-type flip-flops. The first is tied to internal clock phase CLK1 by a compensating delay line, and the second is tied to CLK1 of the second 8182A. An output pulse, whose width is determined by propagation delay feedback, is generated when the second flip-flop is clocked. Clock phases CLK2 of both 8182As then have the same delay with respect to the incoming clock within a few hundred picoseconds, the sampling point delays being different.

Each 8182A's trigger event is sent to the other 8182A (IT in Fig. 14) after being sampled by CLK2. The received trigger signal RT and internally detected trigger signal IT are combined in an AND gate. If triggers are detected in both 8182As, the trigger delay counters are started in parallel. For correct single-analyzer operation, the high-speed line receiver for the twin trigger signal is dc-biased so that its input is always true when no twin interconnections are present.

There are no interconnections between the microprocessors during twin operation, so the selection of any key other than **RUN** and **STOP** on one instrument has no effect on the other. When the **RUN** key is pressed, the microprocessor in that instrument sends an arming signal. The other microprocessor reads this signal and sends its own arming signal in return. When both sent and received arming signals become true, both 8182As go into an armed status simultaneously.

The stop function is achieved simply by OR-gating the

stop signals of both machines.

In the comparator mode, only clock phase CLK1 is used, so the clock arbiter is not required. Trigger word detection and combinational functions are performed by the same elements as in the logic analyzer modes.

Reference

1. J.A. Scharrer, R.G. Wickliff, Jr., and W.D. Martin, "Interactive Logic State and Timing Analyses for Tracking Down Problems in Digital Systems," Hewlett-Packard Journal, Vol. 29, no. 6, February 1978.

Data Analyzer Software/Firmware Design

by Roberto Mottola and Eckhard Paul

LOCAL PROGRAMMING of the 8182A Data Analyzer is done by means of front-panel softkeys. As selections are made, the functions of the softkeys change and are displayed on the CRT. The programming concept provides eight pages of information, four pages for programming instrument parameters, three for displaying the results of a measurement, and an eighth page for use as an alphanumeric display to aid the operator a of computer-controlled system.

For remote programming, the 8182A is provided with an HP-IB (IEEE 488) interface, giving it two remote operating modes, ASCII and binary, with different addresses. The binary mode is intended for fast transfers of binary data to and from the expected data and received data sections of the memory. The contents of the expected data section can be transferred in 320 ms. The memory section (expected or received data), the start address, and whether the 8182A is to send or receive the data can be selected via an HP-IB command in ASCII mode. In ASCII mode, each data byte transferred via the HP-IB is treated as a seven-bit ASCII character. If the 8182A has been addressed as a listener in ASCII mode, the data parameters and mode settings may be changed by sending the appropriate HP-IB command (a sequence of ASCII characters). All commands start with a header which consists of three characters. A real number, an integer, or a formatted entry may follow.

Any HP-IB command can be transferred regardless of the 8182A's status, whether it be idle, armed, or active. Some parameters (e.g., thresholds) can be programmed on the fly, that is the measurement currently being performed is not interrupted. A measurement is only interrupted or aborted if the 8182A is unable to program a parameter on the fly, or if it is impractical to continue the current measurement (e.g, the operating mode has been changed). The commands received via the HP-IB are stored in a 256-byte buffer. When the first character has been stored in the buffer and the main program has time, the main program begins to interpret characters stored in the buffer. Recognized commands are executed. It is unnecessary for the HP-IB controller (e.g., a computer) to wait until each command has been interpreted before sending another, because the storing of characters in the buffer is a priority operation.

To achieve synchronization between the controller and the instrument, a holdoff handshake has been implemented. The 8182A holds off the HP-IB handshake when the controller sends a synchronizing character, thus temporarily halting execution of the controller's program. The holdoff is released when all bytes in the buffer have been interpreted, all recognized commands executed, and the hardware settled. For this reason no WAIT statements are necessary when programming the controller.

The following example is based on an 8180A Data Generator with HP-IB address 7, connected to the 8182A. The programmable synchronizing character defaults to ⟨CR⟩, carriage return.

Output 703; "run"	Starts the 8182A Analyzer
Output 707; "run"	Starts the 8180A Generator

Because a ⟨CR⟩⟨LF⟩ (carriage return, line feed) sequence is normally transferred at the end of each Output statement, the controller executes the second statement in the example only after the 8182A has executed the RUN command. Thus the generator cannot be started before the analyzer has been set to capture data.

When the 8182A has been addressed as talker, it sends status information, current parameter settings, received or expected data, error information, or the contents of the display, depending upon the talker mode. The nine talker modes are programmable by HP-IB commands.

Also available is a status byte, which is read out via the HP-IB after a serial poll has been sent by the controller. The status byte contains the following status and error information:

- HP-IB command either not recognized by interpreter, or not allowed at this time
- Attempt to program an erroneous value via the HP-IB
- Context autocorrection made
- SRQ key pressed
- Stop routine executed
- Fast clock detected
- RQS (Request Service. See IEC 625.1)
- Power-on self-test failed.

The 8182A can also generate a service request to interrupt the controller to inform it that a measurement has been completed.

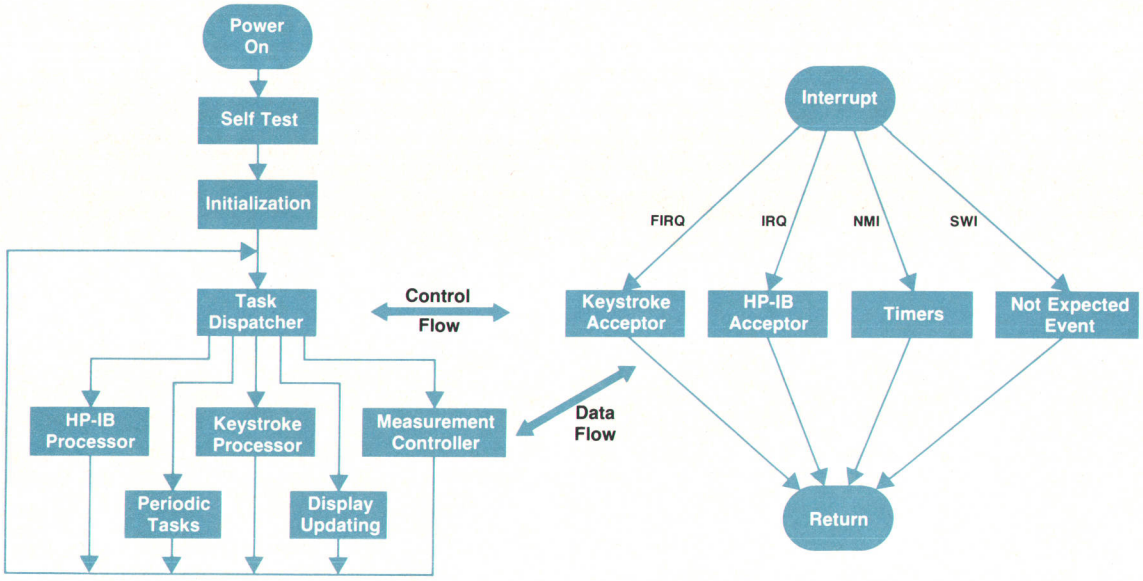

Fig. 1. *The 8182A Data Analyzer main program resembles a real-time multitask operating system. A skilled task dispatcher makes full use of the interrupt structure of the CPU.*

Program Architecture

The structure of the program controlling the 8182A is designed to obtain good performance from the 8-bit microprocessor under varying load conditions. The goal was to guarantee no loss of commands and a prompt response, even in extreme situations. For example, the 8182A might be continuously displaying new data from a repetitive measurement with the operator varying some parameter using a vernier key, while simultaneously logging the whole process on a computer using the HP-IB local talker capability.

The program is designed around a skilled task dispatcher, which makes full use of the interrupt structure of the 6809 CPU. The resulting structure closely resembles the nucleus of a simple real-time multitask operating system. As illustrated in Fig. 1, five tasks are performed by the dispatcher. It uses a mixture of fixed priority and first come, first served queue structures to select from competing tasks.

Priorities are dynamically variable, that is, the program has the ability to decide when a task is becoming gradually more important and requires extra attention, or when a task can be delayed to conserve CPU resources. This feature allows it to adapt to a wide range of controller speeds and different operating conditions (perhaps a lot of display activity, or a CPU-intensive measurement).

The dispatcher also has the ability to recognize when the operator or controller are sending commands that would cause multiple repetitions of the same action. This situation is flagged when recognized, and the action is executed only once at the last possible moment.

The primary function of the interrupt structure is to interface the dispatcher to the outside world. This is made possible via the keystroke and HP-IB acceptor routines. The respective routines react to the asynchronous stimuli from local or remote commands sent to the processor. A routine checks the commands, then communicates with the dispatcher, which is responsible for further processing. The synchronization of different processes is assured by control signals between the acceptors and the dispatcher, data being exchanged between them in global areas.

The NMI line of the 6809 is connected to a 10-ms-period time base which triggers the TIMERS module. This module generates eight programmable delay timers and consumes roughly 5% of the total CPU time. The dispatcher uses the delay timers to perform time-related actions that have to be independent of the CPU load, and to supply timing information to the dynamic priority algorithm.

Keystroke Operation

The keystroke handler and keystroke processor routines together manipulate all the commands entered into the 8182A via the front-panel keypad (local commands). In the event of no local activity, a simple circuit monitors the keypad. If any key is pressed, an FIRQ interrupt, which calls up the acceptor routine, is generated. The acceptor is responsible for keyboard scanning and debouncing the mechanical switches. If a key operation is recognized as valid, the message is placed in a first in, first out (FIFO) buffer, and the dispatcher is told to activate the keystroke processor. The acceptor routine is then complete.

The eight-key FIFO buffer, combined with the interrupt operation, ensures that key action is never lost, even in the case of a heavy CPU load. When the processor takes more time to complete its task the user may perceive a small delay between giving a command and getting a response. The keystroke data is taken from the FIFO buffer by the processor. Different processes are selected and triggered from here depending on the program status and the key function. Typical actions are control of the softkey menus, programming the hardware, and activating the measurement controller.

By using the TIMERS module, the keystroke processor is also able to reschedule itself periodically when keys calling for an automatic repeat function are selected.

HP-IB Operation

The HP-IB functions are realized with the acceptor and processor routines shown in Fig. 1. The acceptor interrupt routine handles all HP-IB activities, but does not interpret ASCII characters received or execute HP-IB commands. Changes of state or address (local, remote, listener, talker) are recognized and stored in RAM. Characters received are stored in a 256-byte buffer in ASCII mode, or in the desired memory location in binary mode. Upon an interrupt, the acceptor disables itself after a state change or if the receiver buffer is full.

The processor executes the state changes, interprets characters stored in the buffer, executes recognized HP-IB commands, and enables the acceptor when the state changes have been executed, or the receiver buffer is no longer full.

The acceptor-processor structure is designed to handle HP-IB activities very quickly. The acceptor stores characters without interpreting or executing them. A slow controller can send the characters on an interrupt-controlled basis. The processor interprets the characters stored in the buffer interactively.

Measurement Controller

The measurement controller is responsible for all processing related to measurement cycles. The most important activity is the programming of hardware for a RUN, and reading back information generated in the hardware after a STOP.

During measurements, the controller can read information from the hardware as soon as it is generated. This information is also passed to the display updating routines, giving the impression of a real-time instrument.

The controller recognizes when the instrument stops independently of external commands. It also generates the synchronization necessary for twin operation, propagating the run and stop commands to the second 8182A. Using the timers, the measurement controller schedules itself in the case of automatically repeated measurement cycles (autoarming).

Periodic Tasks

Two categories of periodic tasks are recognized by the dispatcher. The first is scheduled every 100 ms. Its primary use is for display activities such as pulsing the clock symbol, flashing warnings, updating counters and so on. The period of 100 ms is sufficient to assure good message visibility during a one-shot function.

The second category includes CPU-intensive tasks having a low priority. These are scheduled every 2.5 seconds to keep the demand for CPU time down to 5% of the total. In this category is a routine that checks the rear-panel settings, allowing reaction to an HP-IB address change or a single-twin change without the necessity of a power-off power-on sequence.

A routine for building a CRC (cyclic redundancy check) signature on the 250 bytes of RAM containing the parameter settings is also called every 2.5 seconds. This routine makes it possible to use a CRC algorithm that gives excellent data protection, but is so complex that it would take too much time to compute the CRC after every data change.

Display Updating

The display updating routines are responsible for writing information to the CRT. Static display changes caused by operator commands and dynamic changes occurring when the instrument is measuring and displaying the incoming results in real time require two different routine categories.

Self-Test

When the 8182A is powered up, it executes six self-test routines. Any error encountered during these routines is displayed as an error message. Tests performed are:

1. RAM/stack test
2. ROM test
3. Keyboard test
4. Clock test
5. Address counter test
6. Data board test.

If tests 1 or 2 fail, the self-test procedure stops because the tested function is vital to the remaining tests. If any of tests 3 to 6 fail, the power-up sequence is stopped after completion of the self-test. The program flow resumes after a stop if the user presses the Continue softkey.

The RAM/stack test performs a read/write check of the RAM stack area, then calculates the 16-bit CRC signature of the remaining RAM, storing it repeatedly throughout the stack area. Possible influences between the stack area and the remaining RAM area are checked by building the signature for the remaining RAM area again and comparing it with the signatures stored in the stack area.

The ROM test calculates the signature for each ROM, compares the value with the corresponding signature in the self-test ROM, and displays the numbers of any ROMs in which the comparison failed.

The keyboard test causes an error message to be displayed if one or more keys are being pressed, or appear to be pressed (indicating a short circuit), during this routine.

The clock test checks all paths a signal may take through the timing circuits as a result of delay and width parameter settings. Errors are recognized in the clock error circuit.

The address counter test simulates clock pulses and reads the state of the address counter at several times to check that pulses have been counted correctly and ensure that every address bit is able to toggle.

The data board test checks the high-speed RAMs and ascertains the number of data boards installed in the instrument.

It is possible to execute further self-test routines by pressing an unlabeled softkey and entering a password via the keyboard. The tests have been implemented for service and diagnostic purposes.

In addition to the self-tests described above, the HP-IB commands MEW (memory write) and JSR (jump subroutine) provide another powerful test facility. With the MEW command, any data can be written into a sequence of RAM addresses. If the data represents 6809 program code, the program can be started via the HP-IB command JSR. In this way, additional test programs can be loaded and executed from a controller via the HP-IB for servicing purposes.

Initialization and Unexpected Events

The initialization block of the 8182A firmware checks the

data stored in the battery-backed RAM for integrity, when selecting between a cold or warm start. It then transfers control to the dispatcher. The unexpected event routine permanently monitors the program flow and some critical data areas to avoid the possibility of a system crash caused by program bugs or a defective RAM.

Developing the Firmware

The 8182A control firmware is based on the microcomputer board equipped with a 6809 CPU. The 64K address space consists of 44K of ROM (only 40K is actually used), 14K of RAM for parameter and data storage, 4K of display RAM, and 2K of memory-mapped I/O space.

The 6809 was found to be the most suitable 8-bit CPU for this application. The powerful command set includes complete stack-relative addressing. The local data space of all procedures is in the stack, giving total separation of code and data as well as reentrant and recursive coding.

The 40K-byte program is written entirely in assembly language to extract maximum power from the small CPU and keep the amount of code to a minimum. Most of the procedures are written as structured code and use standard interfaces to communicate with each other. Some exceptions are made in critical areas. Well known synchronizing methods and data exchanging techniques (flags, semaphores, mailbox, etc.) are used in the multitask area of the program.

Most of the procedures dealing with programming or the displaying of categories of similar information are written as interpreters, working on information tables. The structure of these tables is complex in some cases. For example, the parameter updating procedure derives from its table the command to call itself, and builds a new parameter set in a recursive manner. Another typical example of a table-driven interpreter is the procedure dealing with the softkey menu tree.

Power Supplies for the Stimulus/Response System

by Ulrich Otto and Horst Link

IN DESIGNING POWER SUPPLIES for the 8180A Data Generator, 8181A Extender, and 8182A Data Analyzer, the most important objectives were high load current capability and serviceability within a restricted space.

The sizes of the instrument cabinets were limited by the desire to produce a system suitable for benchtop operation. To accommodate the generator, the analyzer, and perhaps two extenders on a bench, the cabinet dimensions obviously had to be limited.

The card rack in the generator holds eleven printed circuit boards with a spacing of 20 mm between boards. The analyzer has thirteen boards with 17-mm spacing. Because both cabinets also accommodate a CRT display, the space available for power supplies is severely restricted. The outer dimensions for the power supplies were fixed at 254 × 152 × 139 mm.

The high load currents are required especially by the −5.2V rails. In the 8180A Data Generator, the current taken from the −5.2V supply by the Rate ICs alone is approximately 7.1 amperes. The total current demanded of the −5.2V supply is on the order of 18.5 amperes. Furthermore, the numerous output amplifier circuits each demand 5.5W from their +15V and −7.5V supplies. In the 8182A Data Analyzer, the complex ECL logic circuits have a total requirement of some 28 amperes on the −5.2V rail, making this supply the most heavily loaded in the system.

To aid production and serviceability, the decision was made at an early stage to produce modular supplies consisting of plug-in units and boards, and to make the three supplies as similar as possible, if not identical.

It soon became evident that the demands made on the 8182A power supply were unusually heavy, and although the concept of switched-mode-with-flyback was adopted for all three instruments' supplies, fundamental differences exist in the 8182A supply.

Fig. 1 illustrates all of the main functional blocks of the 8180A supply. After rectification (or doubling and rectification, in the case of a 115V ac input), the value of the potential at the switching transistor collector is between 200 and 360V, depending on the line voltage.

Starting Circuit

Fig. 2 shows the schematic diagram of the starting circuit block shown in Fig. 1. A 1000-μF capacitor is charged via the resistive divider until the potential across it reaches 26V. At this point, Z24 becomes conductive and switches on the drive circuit for the transistor switch. Energy is then fed to the control circuit. When the potential across the capacitor has decayed to 12V, the transistor switch is turned off and the circuit is ready to begin a new cycle. If no fault condition is sensed by the control circuit, the power supply begins operation before the end of the first start cycle. If, on the other hand, a fault is detected, the start cycle is repeated at three-second intervals. After the start cycle, all primary

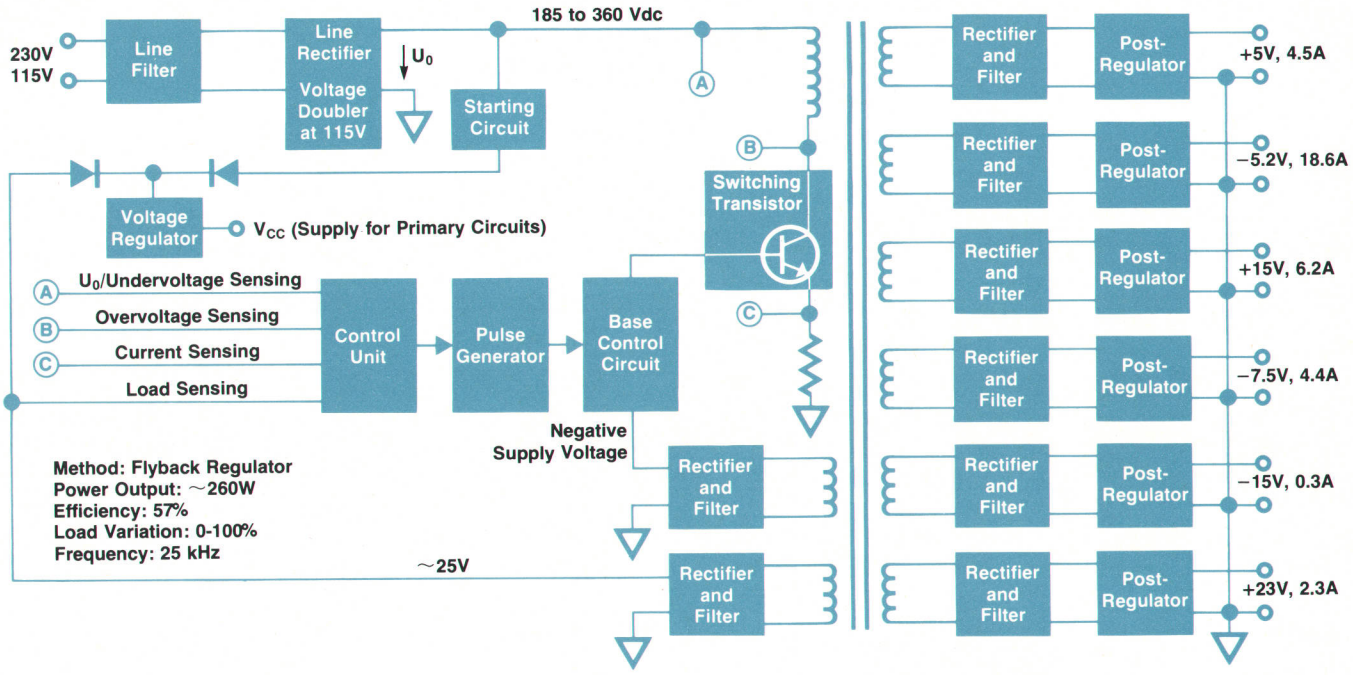

Fig. 1. *Functional block diagram of the 8180A Data Generator power supply.*

circuits in the supply draw their power from the flyback transformer. The normally closed relay contacts remain open, disconnecting the start circuit and conserving power while the instrument is operational.

Control Circuit

A potential of approximately 25V, derived from the transformer, is used to preregulate the power supply. This potential is fed by a divider to the control IC, which establishes the duty cycle. Sensing resistors at various points in the circuit protect components against the following conditions:

- Collector potential of the switching transistor exceeding 1100V
- Rectified line voltage exceeding 370V
- Rectified line voltage falling below 185V
- Switching transistor drawing in excess of 12A.

If the temperature inside the cabinet exceeds 75°C, the switching circuit cuts back its output and supplies a minimum duty cycle. The fan in the power supply continues to run, and all output supplies are shut down.

Switching Transistor

The peak voltage at the collector of the switching transistor is in the order of 1000V. It was therefore necessary to use a component with a very high $V_{(BR)CEO}$ and I_{Cmax}. When the device is negatively biased in its cutoff range, it is possible to attain the 1000V collector-emitter potential. However, during the start cycle, negative voltages are unavailable because of transformer output settling times. Therefore, potentially hazardous situations cannot occur because voltages greater than 700V are not generated during the start cycle, and the transistor adequately handles everything below 700V without being negatively biased.

The positive bias current to the base of the switching transistor is the algebraic sum of the currents from two sources (see Fig. 3). The greater of the two currents (approximately 2.5A) is generated by transforming the 25V primary supply into a pulsed waveform of 6.5V peak to peak. The magnitude of the current is determined by the value of R1. This current goes to the base of the switching transistor via Q1.

The lesser current, 50 mA, is drawn through R2 to the base of Q2. The function of this current is to maintain Q2 in its cutoff state until switch-off occurs. Switch-off is ac-

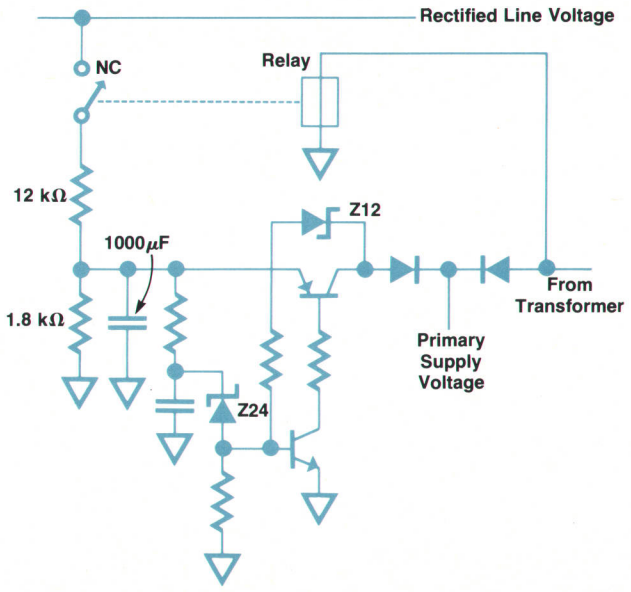

Fig. 2. *Starting circuit schematic diagram.*

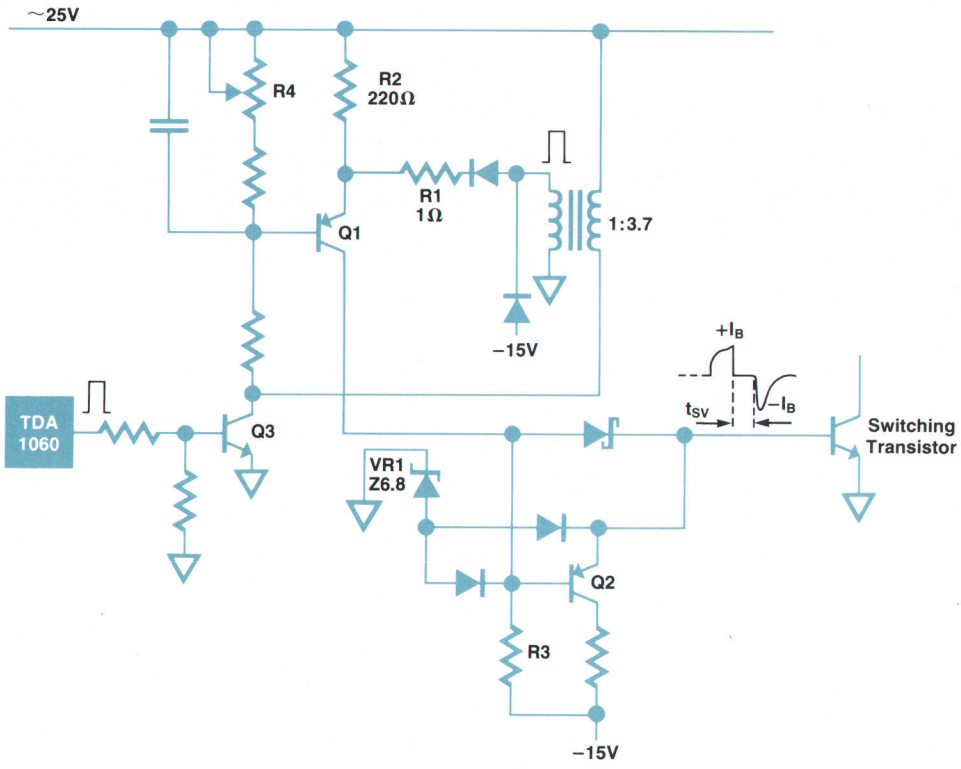

Fig. 3. *Switching transistor base control circuit.*

complished in two stages. In the first, the main component of the bias current at the base of the switching transistor is withdrawn by disabling Q3. The second stage deals with the delayed withdrawal of the lesser component. The delay is achieved by the slow switch-off of Q1, governed by an RC network at the base. R4 allows fine adjustment of the delay time. The result of this delay is that Q2 is maintained in its cutoff state long enough to sink any stored current present at the base-collector junction of the switching transistor. A delay of 2 μs is normally adequate to minimize switching losses.

When the switching transistor is finally turned off, its base potential falls to approximately −7.5V. The cycle is then repeated continuously for as long as the instrument is switched on.

Flyback Transformer

The complex requirements of the power supply, including the number of rails, the high currents, and the total power consumption, made the transformer design a critical concern and especially difficult.

As a starting point, a magnetic core that at the rated power consumption could guarantee an acceptable magnetic flux density of less than 220 mT was required. Another important design criterion was the stray inductance present in the windings, which causes losses in the primary side of the power supply. Furthermore, the triangle current waveforms generated in a flyback system cause a high rms current. This and the skin effect had to be taken into consideration when selecting a material for the windings.

The transformer (see Fig. 4) consists of a U-shaped core with both legs carrying a bobbin, giving a double-width layer. This is of critical importance in dealing with stray inductances. The primary winding is constructed by connecting the windings of both bobbins in series. The secondary windings are sandwiched between two primary winding packages, each having an identical number of turns. All secondary windings are connected in parallel to help deal with high-density currents. These construction methods result in a symmetrical flyback transformer having a stray inductance of less than 3% of the primary inductance.

Further problems concerning high current densities and skin effects were overcome by using multifilar windings of high-frequency stranded wire, each strand having a cross-sectional area of approximately 1.5 mm². Special care in the production of the transformer is necessary because of the numerous bobbin-to-mounting-board connections. Finally, the transformer is encased in a silicone rubber compound.

Postregulators

The 8180A Data Generator power supply provides eight different rails. Six of these are dedicated to satisfying instrument requirements and the remaining two are for sup-

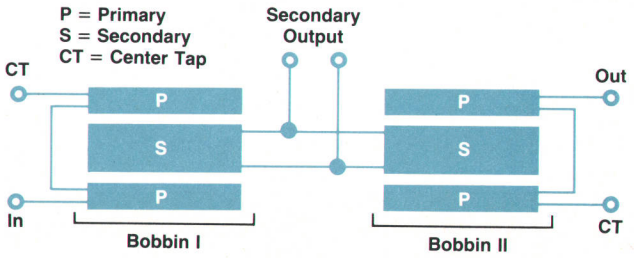

Fig. 4. *Flyback transformer design reduces stray inductance to less than 3% of the primary inductance.*

plying the primary circuits.

The 8180A power supply is also used in the 8181A Extender. In each instrument the internal load varies according to the options supplied. Fine control of the output rails is achieved by postregulators, each of which has its overcurrent sensing circuit.

A transformer sense coil in the primary winding preregulates all supply rails. Preregulation is determined by the efficiency of the secondary voltage that takes the highest loading. In the case of the 8180A, this is the −5.2V rail. If an overcurrent condition occurs at one of the outputs, the common reference voltage for all postregulators is shut off. In turn, all output rails decay to 0V. Because short-duration overcurrents and capacitive loads are present from time to time, shutdown of the output rails is delayed by 70 ms. This, however, results in extra stress on the series transistors in a short-circuit situation. For this reason, if an overload does occur, the postregulators remain down for approximately two seconds, after which the reference voltage comes on again. A check is then made to see if the overload condition still exists, and if so, the reference voltage is again shut off.

8182A Power Supply

Because of the high current demands made on the −5.2V rail, the concept of individually postregulated rails couldn't be implemented in the 8182A because postregulator power losses became unacceptable. To reduce the demands made on the −5.2V rail by the ECL circuits, a −2V supply was implemented. This additional supply permits a saving of over 5A in the −5.2V supply.

A more direct method, in which the duty cycle of the flyback transformer is controlled by an optocoupler, is used in the −5.2V supply. The transformer is designed to allow all rails other than −5.2V to be finely postregulated, as in the 8180A and 8181A. Again, all supplies are protected against short circuits, and if an overload occurs, the power supply is switched off on the primary side by a second optocoupler.

The switch-on phase of the power supply came under close scrutiny. Limited space prevented the use of a line transformer to supply the secondary regulating circuits, so the start cycle is controlled as in the 8180A power supply, using a high-resistance divider for preregulation. As the secondary reference voltage rises, a low-resistance divider fed by the optocoupler is paralleled with the high-resistance divider and takes over control.

Circuitry for regulating the −5.2V rail in the 8182A power supply is very different from that in the 8180A and 8181A. The configuration here consists of a circuit with infinite gain and a very low cutoff frequency. The 100-to-120-Hz ripple cannot be regulated in this circuit, so it is inverted in a low-gain amplifier, then mixed with the −5.2V sense voltage in a unity-gain circuit. The output is then passed to the emitting diode of the optocoupler. The result is a −5.2V supply with a ripple content of less than 30 mV.

New Multi-Frequency LCZ Meters Offer Higher-Speed Impedance Measurements

These instruments, combined with an optional interface and a component handler, make production-line measurements of the impedance parameters of discrete electronic components rapidly and accurately at actual operating frequencies.

by Tomio Wakasugi, Takeshi Kyo, and Toshio Tamamura

MANY INSTRUMENTS used for production-line impedance measurements have only one or two test frequencies, usually 1 kHz and/or 1 MHz. But electronic components, once installed in a piece of equipment, must operate at other frequencies where their parameters can be quite different. Therefore, component users want to measure components at the actual operating frequencies.

Equally important, component manufacturers and end users need low-cost, stand-alone systems capable of high-speed go/no-go measurements without a controller to improve throughput and reduce the cost of production-line testing and incoming inspection of discrete LCR components.

HP's new LCZ Meters, Models 4277A (Fig. 1) and 4276A (Fig. 2), were developed to satisfy these requirements. They can measure eight impedance parameters (L, C, ESR, G, D, Q, $|Z|$, and θ) under a wide variety of test conditions, including variable frequency and dc bias, and can be remotely controlled via the HP-IB (IEEE 488). Features of these two instruments include:

- High speed (see Fig. 3) and high accuracy. Up to 4½-digit-resolution measurements with 0.1% basic accuracy can be done in 70 ms. Fast C-only or L-only measurements are done in 30 ms, and packed binary output sends the measurement data to a controller in 3.4 ms.
- Component measurements at in-circuit operating frequencies. The 4276A measures at 801 frequencies from 100 Hz to 20 kHz and the 4277A measures at 701 frequencies from 10 kHz to 1 MHz.
- Continuous memory. When turned off, or when the power fails, both instruments automatically store all front-panel settings except dc bias and comparator

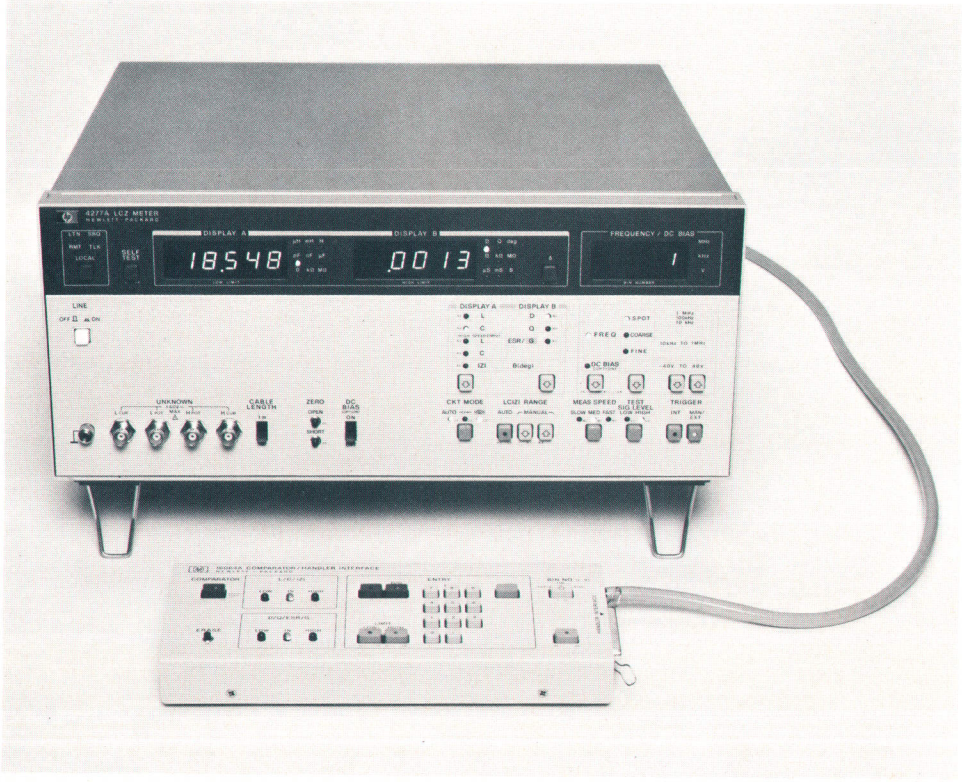

Fig. 1. *The HP 4277A (shown here) and 4276A (Fig. 2) LCZ Meters perform accurate high-speed measurements of impedance parameters of components and materials at frequencies from 100 Hz to 20 kHz (4276A) or 10 kHz to 1 MHz (4277A). By adding an optional comparator/component-handler interface (shown in the foreground), they can be operated in a stand-alone configuration for low-cost, high-speed production-line testing or incoming inspection.*

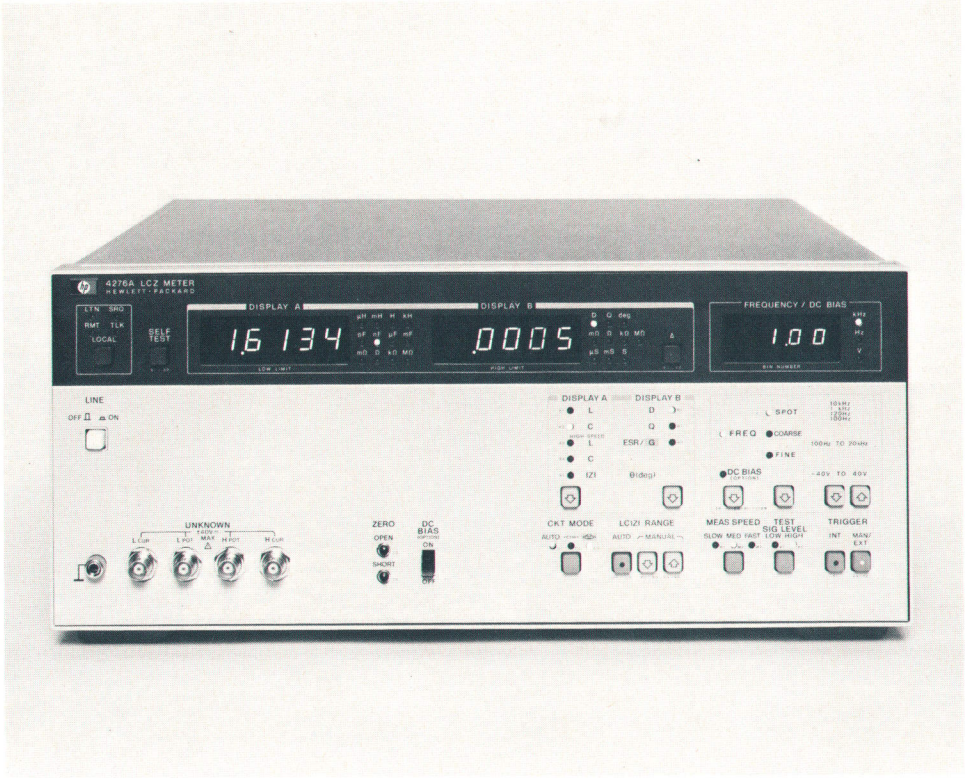

Fig. 2. *HP 4276A LCZ Meter.*

levels.

- dc bias. Measurements can be performed using an external dc bias from 0V to ±40V. An optional internal dc bias source (Option 001) provides the same range of voltages. This internal option is HP-IB programmable with 10-mV resolution from −10V to +10V.
- Two ac signal levels: 1V and 50 mV for the 4276A, and 1V and 20 mV for the 4277A.
- Residual compensation. The residual impedance of the test fixtures and cables can be compensated (up to 20 pF of open-circuit capacitance and 2 ohms of short-circuit resistance).
- Self-test. An automatic built-in functional test verifies proper operation of analog and digital circuits.
- Low cost and high reliability. Thick-film hybrid integrated circuits reduce cost and increase reliability.
- Comparator (Option 002). This option allows a user to set up ten pairs of high/low limits for L, C, and Z and, by adding the HP 16064A keyboard (shown in Fig. 1), control a component handler directly. This interface, which uses optoisolators to provide high noise immunity, can be programmed via the HP-IB.

Design

The major sections of these LCZ meters are the bridge, the vector ratio detector, the oscillator, and the digital circuitry (see Fig. 4). The bridge provides a complex voltage V_x across the device under test (DUT) and another complex voltage V_r which is proportional to the complex current flowing through the DUT as a result of the applied voltage V_x. The vector ratio detector determines the precise complex voltage ratio between V_x and V_r and supplies this information to the digital section for processing and display. The oscillator supplies the excitation to the bridge at frequencies selected by pressing front-panel pushbuttons or by HP-IB commands.

Bridge

Although the bridge sections in the 4276A and 4277A operate in the same way, they use different approaches suitable for covering the different measurement frequency ranges. The bridge section used in the 4277A is the same design as the bridge used in the earlier HP 4274A and 4275A LCR Meters.[1] A modulation technique maintains high gain and stability over the 4277A's full test frequency

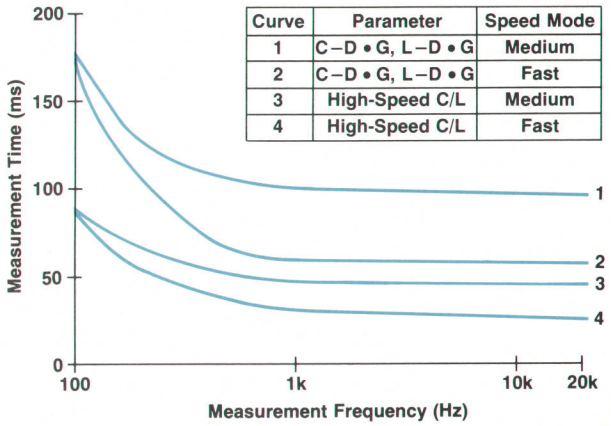

Fig. 3. *Typical high-speed measurement capability of the 4276A for various component parameters as a function of test frequency when the instrument is operated in the AUTO circuit mode.*

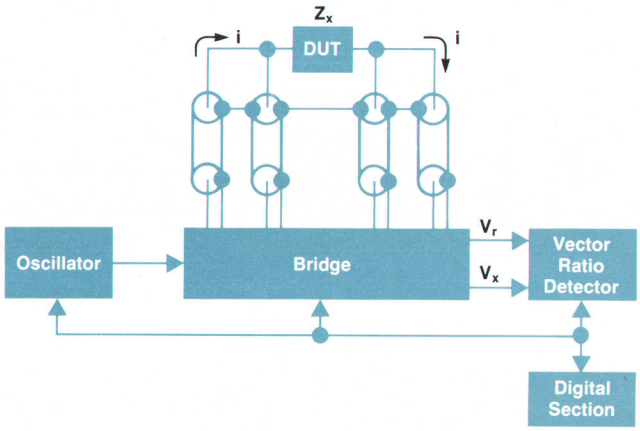

Fig. 4. *Simplified block diagram of 4276A and 4277A LCZ Meters.*

range from 10 kHz to 1 MHz, and a four-terminal pair configuration eliminates errors caused by mutual inductance between cables.

A different design (Fig. 5) is used in the 4276A. Since the test frequency range is lower than that of the 4277A, a simple feed-forward differential amplifier is used for the current-to-voltage converter. This amplifier is designed to maintain high stability for various DUTs and measurement cable lengths. The measurement error in the high-frequency range caused by the reduced gain of this amplifier and the capacitance of the L_{CUR} (low current) and L_{POT} (low potential) cables is compensated by the error correction program in the 4276A's digital section. The connections between the DUT and the 4276A's measurement cables use a five-terminal configuration consisting of H_{CUR}, L_{CUR}, H_{POT}, L_{POT}, and Guard. This configuration eliminates errors caused by mutual inductance between cables because the outer conductors of the H_{CUR} and L_{CUR} cables form a current return path, as in the earlier HP 4274A and 4275A LCR Meters.[1]

In both the 4276A and 4277A, the voltage at the virtual

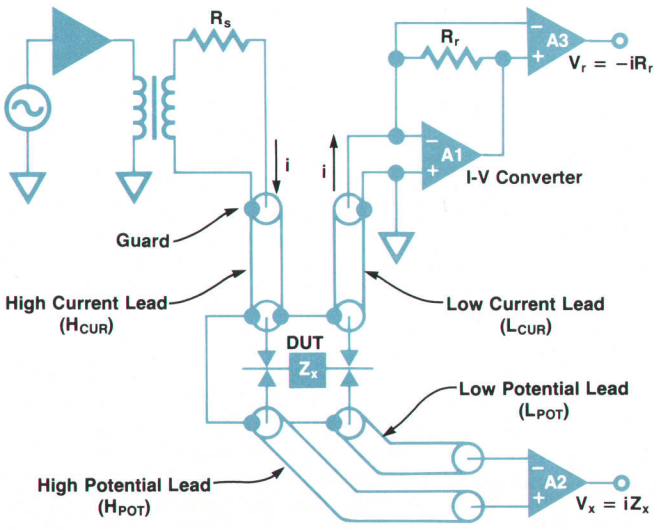

Fig. 5. *Bridge section of the 4276A.*

Comparator

When the 4276A is equipped with the optional comparator (Option 002), a powerful, fully automatic system capable of 10-bin sorting and go/no-go testing can be easily built by connecting a component handler as shown in Fig. 1. Such a system can be operated either with an external controller or, by using the HP 16064A keyboard, without a controller. All comparison information and settings are accessible via the HP-IB (IEEE 488).

To improve sorting speed, two different output signals are available to the component handler, the INDEX signal and the EOM (end-of-measurement) signal. Total measurement time for a component consists of two periods: the time required to do the analog measurement and the time required for the instrument's microprocessor to calculate the results. Many instruments output only an EOM signal when the microprocessor completes its calculations. However, since the device under test (DUT) must be connected to the meter only during the analog measurement period, it can be disconnected during the calculation period and the handler can be moving to the next DUT while the microprocessor is calculating the result. The INDEX signal output by the comparator when the analog measurement is completed allows this, thus increasing measurement speed by subtracting the calculation time. For example, the time per C-D measurement at 1 MHz with the 4277A can be reduced by 20 ms.

This interface has open-collector outputs, so the signal lines can be driven from an internal TTL-level 5V supply (all outputs) or from external voltage supplies up to 30V for decision outputs and 15V for control signals. The control lines—TRIGGER, EOM, and INDEX—are optically isolated to provide ground isolation and prevent false triggering caused by noise.

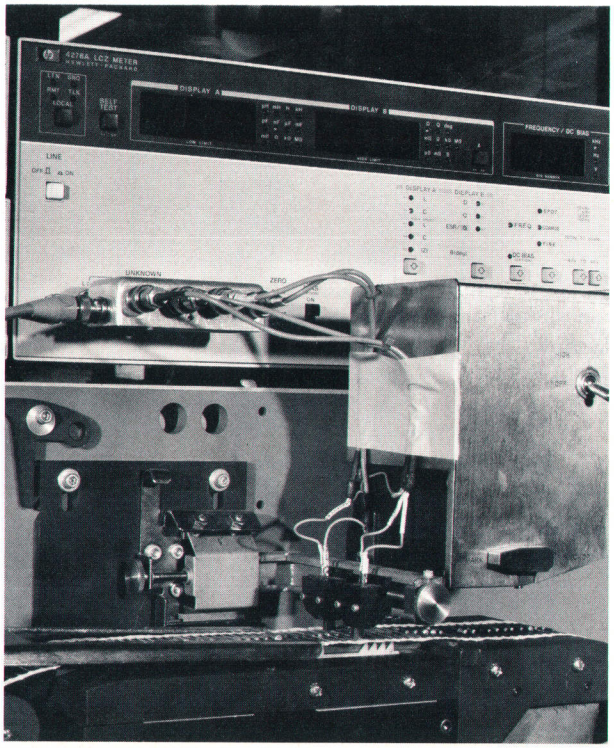

Fig. 1. *Option 002 provides simple go/no-go testing and 10-bin sorting by interfacing a 4276A or 4277A directly to a component handler.*

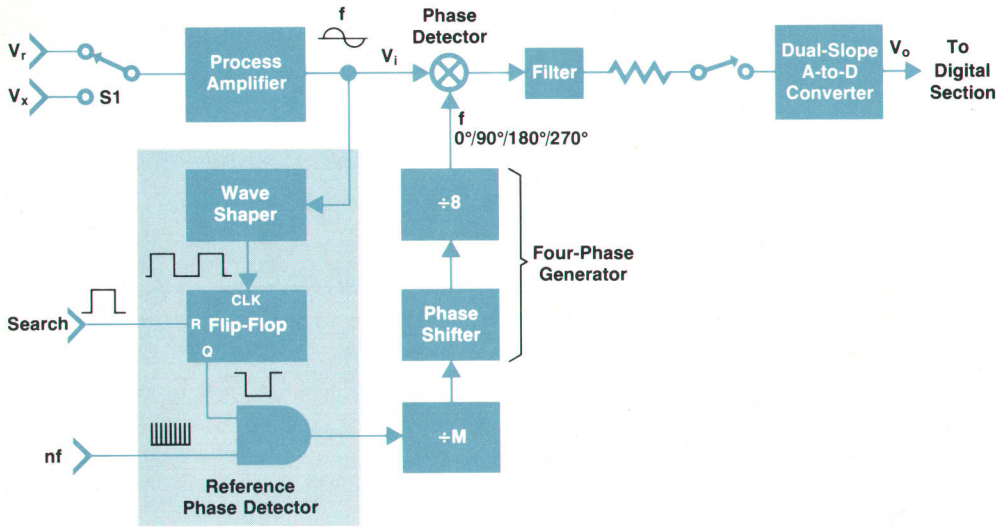

Fig. 6. *Block diagram of the vector ratio detector used in the 4276A and 4277A LCZ Meters.*

ground point (L_{POT}) is zero when the bridges are balanced. Then

$$\frac{V_x}{Z_x} = i = -\frac{V_r}{R_r}$$

Therefore,

$$Z_x = -R_r \frac{V_x}{V_r}$$

Therefore, all that is needed to calculate the complex impedance of the DUT is the value of R_r and the vector ratio between V_x and V_r.

The bridge sections in the 4276A and 4277A are fabricated using custom thick-film hybrid integrated circuits to reduce cost and space.

Vector Ratio Detector

Fig. 6 shows a simplified block diagram of the high-speed vector ratio detector section used in both LCZ meters. This section detects the precise complex voltage ratio between the two signals V_x and V_r from the bridge section. To obtain good tracking characteristics and linearity for various signal levels, the two signals are time-multiplexed by switch S1. The process amplifier block contains attenuators and variable-gain amplifiers to optimize the signal level to the phase detector. The four-phase generator provides the precision 90° phase rotations used to detect the orthogonal components of the input signals to the phase detector.

Fig. 7 is a vector diagram showing V_x, V_r, and the x and y coordinates as determined by the reference phase detector. Here a, b, c, and d are the orthogonal components of V_r and V_x detected by the phase detector and defined in the following equation.

$$\frac{V_x}{V_r} = \frac{c + jd}{a + jb} = \frac{ac + bd}{a^2 + b^2} + j\frac{ad - bc}{a^2 + b^2} = x + jy$$

The vector ratio detector used in the earlier HP 4274A and 4275A LCR Meters requires four integration cycles and two dc reference current sources, and measures the four components a, b, c, and d separately by using dual-slope

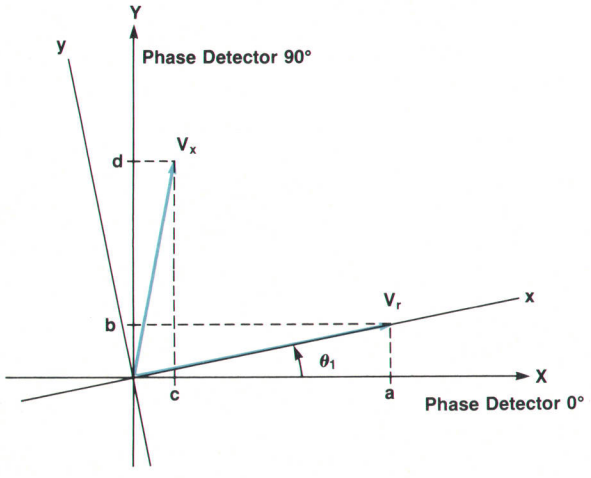

Fig. 7. *Vector diagram showing the orthogonal components of V_x and V_r at the input of the phase detector. θ_1 is the reference phase error.*

Integration Cycle	Period	1		2		3		4	
	Ramp	↗	↘	↗	↘	↗	↘	↗	↘
dc Discharge Method	Measures x + jy	a	k	b	k	c	k	d	k
		V_r 0°	dc	V_r 90°	dc	V_x 0°	dc	V_x 90°	dc
ac Discharge Method	Measures x + jy	b	a	c	a	d	a		
		V_r 90°	V_r 0°	V_x 0°	V_r 0°	V_x 90°	V_r 0°		
	Measures jy only*	d	a						
		V_x 90°	V_r 0°						

*For High-Speed C or L Measurements Only.

Fig. 8. *Comparison of the dc and ac discharge methods for determining the orthogonal components a, b, c, and d of the voltages V_x and V_r.*

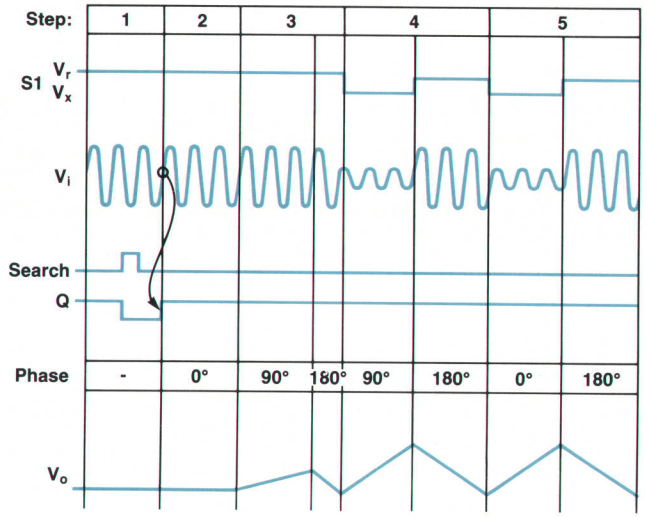

Fig. 9. *Measurement sequence for the vector ratio detector. The steps are 1) reference phase detection, 2) autozero, 3) first A-to-D conversion for α, 4) second A-to-D conversion for β, and 5) third A-to-D conversion for γ. In the reference phase detection step, the output signal Q of the flip-flop (see Fig. 6) goes high coincidentally with the zero-crossing point of V_i, thus detecting the reference phase 0°*

analog-to-digital conversion (dc discharge method).[1] To improve measurement speed, the dual-slope analog-to-digital converter in the 4276A and 4277A measures the scalar ratio between two components directly without any dc reference source (ac discharge method). This increases measurement speed by eliminating one integration cycle and reduces cost by eliminating the dc reference sources. If only the reactive component of impedance is measured, the ac discharge method requires only one integration cycle, further increasing measurement speed. Fig. 8 shows the difference in steps between the two methods.

The vector ratio x + jy is calculated as

$$x = \frac{ac + bd}{a^2 + b^2} = \frac{\gamma + \alpha\beta}{1 + \alpha^2}$$

and

$$y = \frac{ad - bc}{a^2 + b^2} = \frac{\beta - \alpha\gamma}{1 + \alpha^2}$$

where $\alpha = b/a$, $\beta = d/a$, and $\gamma = c/a$. Then the unknown impedance Z_x is given by

$$Z_x = -R_r(x + jy) = -R_r\left[\frac{\gamma + \alpha\beta}{1 + \alpha^2} + j\frac{\beta - \alpha\gamma}{1 + \alpha^2}\right] \quad (1)$$

The measurement sequence of the vector ratio detector consists of five steps which include reference phase detection and autozeroing (see Fig. 9). The reference phase detector is used to minimize the reference phase error θ_1 (Fig. 7). Since the discharge period of the first integration cycle is proportional to θ_1, reducing θ_1 reduces measurement time.

To minimize θ_1, reference phase detection in the 4276A uses high-speed clock signals (nf) which are multiples of the test frequencies (see Fig. 6). The 4277A uses the same automatic phase adjust technique used in the 4261A LCR Meter.[2]

For high-speed inductance or capacitance measurements, only $\beta = d/a$ is detected. Equation (1) implies that when the reference phase error θ_1 is negligible (i.e., $\alpha = b/a$ is very small), the unknown impedance Z_x is approximately equal to $-R_r(\gamma + j\beta)$. Thus the unknown reactance is simply obtained by dividing or multiplying by the factor $2\pi f$.

The phase-detected signal of Fig. 6 has to be converted into a dc voltage very quickly for high-speed measurements. In the 4277A, a simple low-pass RC filter is used to reject the ripple component of the phase-detected signal. However, the 4276A's lower frequency range requires a different approach. The low-pass RC filter, which would have too long a settling time at the lower frequencies, is replaced by a preintegrator (Fig. 10) whose integration time is equal to a multiple of the test signal period. Therefore, the output V_o is exactly proportional to the dc component of the input signal. Thus, even at the lowest frequency of 100 Hz,

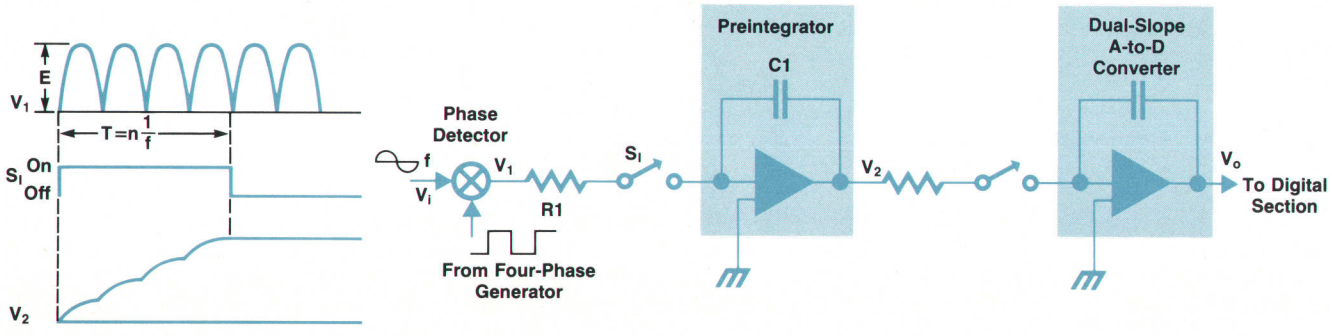

Fig. 10. *A preintegrator is used in the 4276A's vector ratio detector to convert the phase-detected signal to a dc voltage precisely proportional to the dc component of the input signal.*

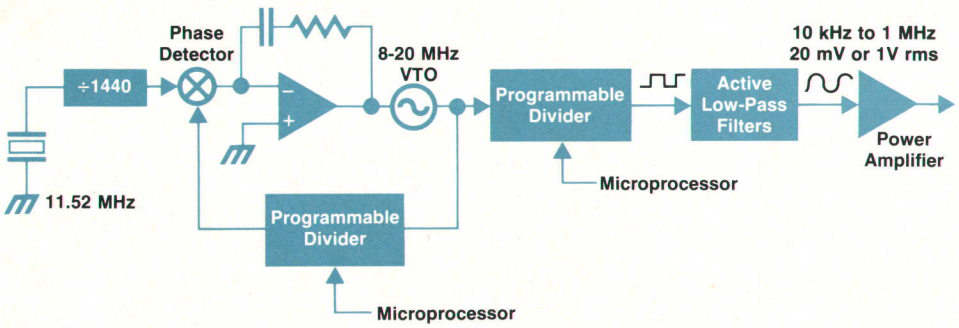

Fig. 11. *Block diagram of the signal source used in the 4277A LCZ Meter.*

only one test signal period of 10 ms is needed for the conversion.

Oscillator

The signal source in the 4277A contains an 11.52-MHz crystal oscillator, a conventional phase-locked loop, programmable dividers, a voltage-tuned oscillator (VTO), and an active low-pass filter output stage. This circuit, illustrated in Fig. 11 by a simplified block diagram, outputs a 10-kHz-to-1-MHz sine wave with 2½-digit frequency resolution. The output filter consists of four active low-pass filters that convert the square-wave output of the programmable divider into the required sine wave. Each low-pass filter is realized in the form of a specially designed hybrid circuit. Feedback is used to shift the cutoff frequency of the filter to the fundamental frequency of the square-wave input. Total harmonic distortion of the output sine wave is less than 60 dB over the 10 kHz to 1 MHz range.

Digital Section

The digital section is based on a Z80B microprocessor clocked by a 6-MHz quartz oscillator. All of the high-speed measurement calculations including error correction, data control, and analog control are handled by this section in addition to controlling the display and interfacing to the front-panel and the HP-IB. A battery-powered memory stores all front-panel settings except dc bias, the open-circuit and short-circuit zero offset values, and reference values for deviation measurement for approximately two weeks after the instrument is turned off or power fails.

High-Speed Programmable dc Bias Options

To evaluate varactor diodes or MOS devices, high-speed measurement of capacitance at a number of dc bias levels is essential. These measurements are usually performed with an external dc source controlled by a computer, but the H03 and H04 options for the 4277A offer an inexpensive and simple solution to this requirement.

The only differences between the two options are the test signal levels. The H03 option supplies 20-mV and 1V signal levels, and the H04 option supplies 20-mV and 500-mV levels, which are better suited for varactor testing. Both options use an HP-IB programmable dc bias source and operate at 1 MHz. Other common features include an automatic bias sweep, packed binary data transfer, short settling times, and selectable delay.

Typical operation begins with the H03 or H04 4277A accepting and memorizing up to 31 dc bias points from the HP-IB before starting measurement. Upon receiving the measurement trigger signal, the instrument begins its sweep, makes a measurement at each preprogrammed dc bias level, and stores the measurement data in its buffer memory. When the sweep is completed, the stored data is dumped to the computer through the HP-IB in packed binary format.

With these options, measurement speed is 1.4 times faster than with a standard 4277A because the settling time for dc bias is 25% faster, and the settling times for function, ranging, and signal level are 50% faster. For example, the capacitance for ten dc bias levels can be measured in approximately 450 ms (see Fig. 1).

In addition, because the automatic bias sweep eliminates the need for handshaking to set dc bias and to trigger measurements during a sweep, one computer can control several H03 or H04 4277As through timesharing.

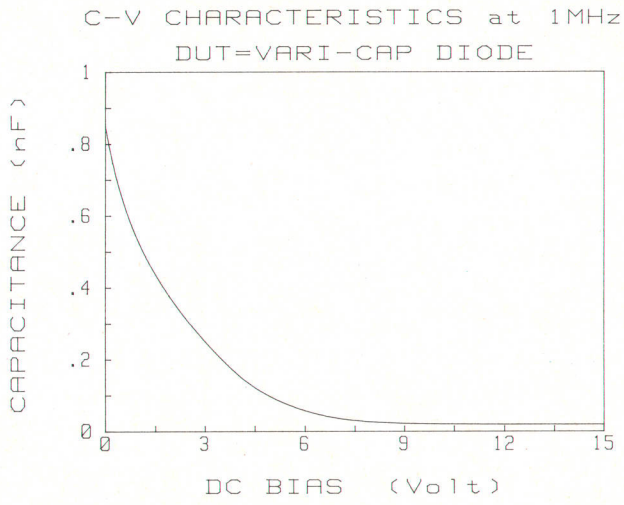

Fig. 1. *The C-V characteristics of a varactor diode at 10 dc bias points can be measured in approximately 450 ms using a 4277A LCZ Meter equipped with an H03 option.*

Acknowledgments

The 4276A and 4277A design team members who deserve special recognition are Noriyuki Sugihara, project manager, Toshio Ichino, Katsushi Aoki, and Masayoshi Habu, analog section, Satoru Hashimoto, digital section, Kiyoshi Suzuki, power supply, Kenji Shimada, self-test system, Hiroshi Shiratori and Tetsuya Shiraishi, mechanical design, and Tsuneji Nakayasu, industrial design. Special thanks also to Takeo Shimizu for his general management and encouragement.

Besides those mentioned above, many other people including Seiichi Kikuta, Kohichi Yanagawa, and Hideki Wakamatsu made significant contributions to the project. Our thanks to them too.

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1. K. Maeda and Y. Narimatsu, "Multi-Frequency LCR Meters Test Components under Realistic Conditions," Hewlett-Packard Journal, Vol. 30, no. 2, February 1979.

2. S. Hashimoto and T. Tamamura, "An Automatic Wide-Range Digital LCR Meter," Hewlett-Packard Journal, Vol. 28, no. 1, September 1976.

History from the Pages of the Hewlett-Packard Journal

More than a year ago, Roberto Albanesi, Hewlett-Packard's Country Manager in Italy, offered us a suggestion. Why not publish a book of articles from past issues of the HP Journal? Select the articles on the basis that the technologies or products they describe represented significant advances for their time.

The same suggestion later turned up in responses to last year's First HP Journal Reader Opinion Survey. Around here, people seemed to like the idea, and the idea became a project.

Twenty or so knowledgeable HP experts were polled for suggestions of what articles to include. They had thirty-three years of HP Journals to pick from. The final selections were made by William R. Hewlett, HP's cofounder, and Bernard M. Oliver, former vice president for research and development. Mr. Hewlett agreed to write an introduction for the book.

We're now in the last stages of getting the book ready for the printer, so when you read this, it may not be available yet. But look for it, it will be along soon.

The name of the book is "Inventions of Opportunity: Matching Technology with Market Needs." William R. Hewlett's introduction describes the technique of "engineering of opportunity" that guided the company to many successful products, especially in the early days.

Among the articles are those on the first high-speed frequency counter, the HP-35 Calculator that replaced the slide rule in engineers' pockets, the beginnings of computer-controlled instrumentation systems, and many others. The introduction comments on each article, providing insights into the dynamics of innovation and showing how a need, a technology, and creative people come together to produce a successful invention.

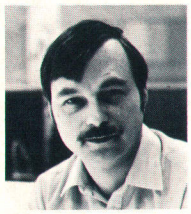
The book is cloth-bound, has a dust cover, and contains more than 350 pages. It will be obtainable through HP sales offices around the world, or through HP's computer supplies telephone order service, which is available in many countries. The book has an HP part number: 92233B. The cost will be modest.

-R.P. Dolan

Authors

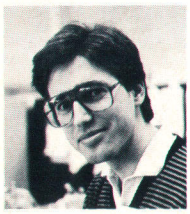
July 1983

Klaus-Peter Behrens



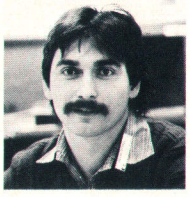
Klaus-Peter joined Böblingen Instruments Division in 1978 after receiving his engineering diploma from the University of Stuttgart. He was responsible for the design of the software and digital control in the 8180A Data Generator and the 8181A Data Generator Extender. Klaus-Peter is married and lives in Böblingen. In his spare time he builds model railways.

Andreas Wilbs



Andreas Wilbs was born in 1953 in Heilbronn, West Germany. He joined HP in 1980 as a sales support engineer for logic signal sources, and since 1981 has been a product marketing engineer. He designed the specialist training package for the 8180A/81A/82A and is responsible for the system's post-introduction activities. Andreas is married and enjoys all kinds of outside activities including portable video recording.

Werner Berkel



Werner Berkel was born in Speyer and attended school in Karlsruhe, where he received his degree in 1979. He contributed to the design of the 8180A and supervised the design of the 15413A Tri-State Unit and the 15414A Tri-State Pod. Werner enjoys music, soccer, and table tennis. He is married and lives in Böblingen.

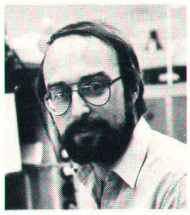
Ulrich Hübner

Born and raised in Stuttgart, Ulrich Hübner studied at the technical universities of Aachen and Stuttgart. He joined HP's Böblingen Medical Division in 1967, then moved to the instrument lab, where he developed low-cost oscilloscopes. He was responsible for the hardware design of the 8170A Logic Pattern Generator, then served as project manager for the 8180A/8181A Data Generator. Ulrich is married, has one child, and enjoys swimming and skiing in his spare time.

Josef Becker

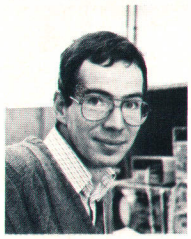
Jo Becker joined HP towards the end of 1979, having previously worked at the University of Stuttgart as a biomedical engineer. He was responsible for the design of the 8180A Data Generator output amplifiers, and has now moved to the fiber optics group at HP's Böblingen Instruments Division, where he is involved in the development of detector heads. Jo is married and has three sons. His hobbies include amateur radio and astronomy.

Heinz Nüssle



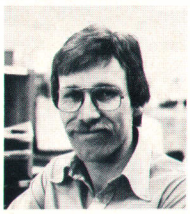
Heinz Nüssle was born in Böblingen and came to HP as an apprentice in 1967. After his apprenticeship, he studied at the University of Stuttgart, where he gained his engineering degree in 1980. In 1981 he returned to HP and contributed to the design of the 8180A Data Generator and the development of the 15413A/15414A Tri-State Unit and Pod. Heinz is a member of the German Red Cross and enjoys white-water kayaking.

Ulrich Schöttmer



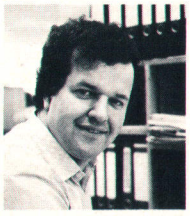
Ulrich Schöttmer joined HP in 1981, and has contributed to the high-speed digital control of the 8182A Data Analyzer. He received his engineering degree at the University of Bochum. Ulrich lives in Böblingen and enjoys radio-controlled aircraft and skiing.

Martin Dietze



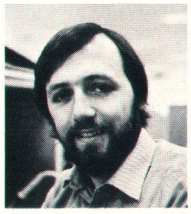
Martin Dietze has been a project engineer with HP since 1980. He received his engineering degree from the University of Stuttgart in 1979. Martin was involved in the development of the 8182A Data Analyzer and designed the high-speed counters and glitch detectors. Born in Leipzig and now a resident of Böblingen, Martin enjoys traveling, backpacking, cycling, and playing the violincello.

Dieter Kible



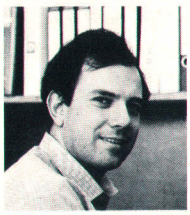
Dieter Kible was born near Lake Constance, and graduated from the University of Stuttgart in 1975. He joined HP shortly afterwards, contributing to hardware and software design of the 8165A Programmable Signal Source. He has been project leader for the 8182A Data Analyzer since 1978. Dieter is a member of DKE, the German counterpart of the IEC, working on instrument bus systems. He is married, has two sons, and spends much of his spare time working on his house and playing tennis and cards.

Bernhard Roth



Born and raised near Lake Constance, Bernhard earned his degree at Ulm in 1978. He joined HP the same year, and began work on the 8182A Data Analyzer. He designed the active probe, input amplifiers, clock timing circuits, and log voltage generator for that instrument. A member of the HP table tennis team, he is single and enjoys rock music concerts and motion pictures.

Roberto Mottola



Roberto Mottola is a native of Italy, and attended the University of Trieste, graduating in 1976. He moved to Germany and joined HP in 1979, after three years of research in digital image processing. Roberto developed the operating concept for the 8180A/81A/82A Data Generator and Analyzer system, and part of the 8182A control program. He is married and has two children. He spends his spare time with his family, swimming, listening to classical music, and building a model railway.

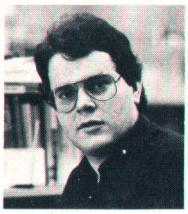
Eckhard Paul

Eckhard Paul was born near Flensburg in Northern Germany, and graduated from the Fachhochschule of Kiel in 1981. He joined HP the same year and has been responsible for the HP-IB and self-test software in the 8182A Data Analyzer. Eckhard is unmarried, and enjoys playing cards, skiing, camping, and cycling.

Horst Link

Horst Link joined HP in 1970, and spent his early years on the mechanical design of tape punches and readers for calculators and data acquisition systems. He later became responsible for the mechanical design of various pulse and data generator mainframes and modules for use in 1-GHz pulse generators and the 8170A Logic Pattern Generator. Horst is married, has a ten-year old daughter and lives in Böblingen. He spends much of his free time working around his house and hiking. He is also an accomplished photographer.

Ulrich Otto



Ulrich Otto joined HP in 1979. He was responsible for the design of the power supplies for the 8180A, 8181A, and 8182A. He received his BSEE from the School of Engineering in Esslingen in 1976, and went on to gain his MSEE at the University of Stuttgart. A native of Stuttgart, Ulrich now lives in Ehningen, near Böblingen. He enjoys tennis, swimming, running, and reading, and spends much of his spare time hiking in the mountains in summer and downhill skiing in the winter.

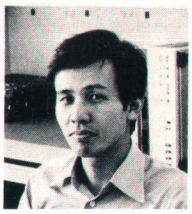
Takeshi Kyo

Takeshi Kyo joined Yokogawa-Hewlett-Packard in 1970 after receiving his BEE degree from Iwate University. He contributed to the design of the 4271A 1-MHz LCR Meter and the 4274A and 4275A LCR Meters. He developed the software for the 4276A and 4277A LCZ Meters. He is married, has one daughter, and enjoys skiing and playing GO, a Japanese game similar to chess.

Toshio Tamamura

Since joining Yokogawa-Hewlett-Packard in 1971, Toshio Tamamura has been a principal contributor to the design of several HP LCR meters. He developed the analog section circuitry for the 4277A LCZ Meter and designed some of the hybrid integrated circuits. He has a BSEE degree received in 1971 from the University of Electro-Communications. He is married and the father of two children, and likes playing tennis.

Tomio Wakasugi



After graduating with a BSEE degree from Waseda University in 1976, Tomio Wakasugi worked for three years in telecommunications before joining Yokogawa-Hewlett-Packard in 1979. He worked on the 4192A LF impedance Analyzer and designed the self-test systems for the 4193A Vector Impedance Meter. He designed the analog section for the 4276A LCZ Meter. Besides being captain of YHP's volleyball team, his interests include tennis, jazz, and amateur radio.

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